Robust and Cost Effective Synchronization Scheme for a Multicell Grid Emulator

N. Hildebrandt, M. Luo, and D. Dujic

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Robust and Cost Effective Synchronization Scheme for a Multicell Grid Emulator

Nicolai Hildebrandt, Student Member, IEEE, Min Luo, Member, IEEE, and Drazen Dujic, Senior Member, IEEE

Abstract—Steadily increasing requirements for grid connected converters, their growing unit power and output voltage call for flexible high-power medium-voltage grid emulators. Four-quadrant cascaded H-bridge topology features high output voltage resolution and high effective switching frequency which enable high-dynamic high-fidelity grid emulation. This paper shows that despite non-idealities (turn ratios, phase-shift angles and different stray inductances) in a typical phase-shifting multiwinding transformer, active front-ends of the cells can be effectively synchronized to their respective supply voltages using transformer primary side voltage measurements and nameplate values. Consequently, cell input filters can be omitted, making the grid emulator more compact, cheaper, faster and exhibiting more robust grid synchronization. Theoretical developments and designs are verified by means of high fidelity time domain simulations.

Index Terms—Grid emulator, cascaded H-bridge converter, phase-shifting multiwinding transformer, grid synchronization, phase-locked loop

NOMENCLATURE

Superscripts

* reference value
p transformer primary side
s transformer secondary side

Subscripts

abc three-phase components
dq synchronous reference frame components
αβ stationary reference frame components
nom nominal value
LL line to line
LN line to (real or virtual) neutral

I. INTRODUCTION

Two main trends could be observed in the domain of renewable energy sources over the last two decades: I) the generator and Grid-Connected Converter (GCC) size have been steadily growing towards the double-digit barrier of 10 MW [1] and crossed the line between Low Voltage (LV) and Medium-Voltage (MV) technology to further increase their power density [2], [3], and II) with higher renewable energy penetration, power system operators repeatedly increased requirements for GCCs [4] which fulfillment consequently needs to be verified during the GCC certification process.

While widely available for LV, high-bandwidth converter based grid emulators that offer full flexibility in testing of GCCs are still very rare at MV high-power level [5]–[9] despite the growing need. One of the promising topologies for this application is the Cascaded H-Bridge (CHB) topology depicted in Fig. 1 with first MV megawatt class projects at TECO-Westinghouse Motor Company, USA [8], Xi’an Jiaotong University, China [9] and EPFL, Switzerland [10].

The MV output stage of the CHB topology features a high resolution multilevel output voltage at a high effective output switching frequency. This is achieved by the series connection of N H-bridge inverter cells per phase [11] that results in \(2N+1\) voltage levels and \(N\) times higher apparent switching frequency than the cell switching frequency if the \(N\) carriers are evenly interleaved [12]. Furthermore, LV semiconductors can be switched significantly faster than their MV counterparts, especially if considering LV SiC based power semiconductor devices for the output stage. This enables a high cut-off frequency MV output filter that allows to emulate high-order harmonics and fast transients [10].

While the projects [8], [9] utilize wye-delta type transformers to supply three to nine power converter cells per transformer, a commercial phase-shifting transformer with 15 secondaries shown in Fig. 2 with parameters listed in Table I is used in this paper. These phase-shifts result from its
As shown in Fig. 3, a typical bidirectional CHB cell would feature an input filter [14], be it damped $CL$ [15]–[18] or $LCL$ filter [9] or just an $L$ filter [19] which is most common practice, with its inductance required for the AFE operation. These AFE filters take a significant share of a cell’s volume, weight, cost and cooling effort or require separate cabinets. There is a strong incentive to avoid these discrete filters, not only for the direct capital costs of the grid emulator but also for the operating costs in a high-power medium-voltage laboratory where floor space and cooling infrastructure is expensive.

We therefore demonstrate that a bidirectional grid emulator based on CHB topology and a phase-shifting Multiwinding Transformer (MWT) can be operated without presence of any discrete filtering structure between transformer secondary windings and each bidirectional cell. The results presented in the paper show that the grid synchronization and AFE control can be implemented with improved transient response and a high level of robustness against this variation of transformer parameter values using a simple Phase-Locked Loop (PLL) and the same set of control parameters for all cells, as it is desired in a modular design. In contrast to the MV drive application [20], CHB based grid emulator cell AFEs need to stabilize dc link voltages during very fast power transients, whereby the MWT behaves far from ideal, and ensure sinusoidal supply grid currents during asymmetric loading.

In this paper, Section II explains the high dynamics requirements for the cell supplies in a grid emulator application, Section III presents the MWT characteristics, Section IV describes the synchronization schemes. Section V compares their performances, followed by the Conclusion.

### II. Dynamics in a CHB Based MV Grid Emulator

In its most basic function, a grid emulator serves as a flexibly programmable and stiff voltage source that can reproduce grid voltage waveforms of desired amplitude, frequency and phase for nominal and distorted conditions or grid faults as they can appear during real grid operation. Ability to reproduce high order harmonics and grid faults sets high requirements for the grid emulator output stage control dynamics. In a cell where the AFE regulates the dc link voltage, the emulated grid fault produces the strongest disturbance for its control.

Fig. 4 illustrates the output voltage curves during a short emulated grid fault while the converter under test feeds constant load during this disturbance. The fault is applied at zero grid frequency and alternates between line faults of different phases. The converter under test is not allowed to respond to the fault, i.e., it is not allowed to do any power control actions during the fault period.

**TABLE I**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Apparent Power Rating</td>
<td>1 MVA</td>
</tr>
<tr>
<td>Short-Circuit Impedance</td>
<td>7.8%</td>
</tr>
<tr>
<td>Primary / Secondary Side Line Voltage</td>
<td>6 kV / 676 V</td>
</tr>
<tr>
<td>Grid Frequency</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Star Primary Windings</td>
<td>1</td>
</tr>
<tr>
<td>Extended Delta Secondary Windings</td>
<td>15</td>
</tr>
<tr>
<td>Phase Shifts of the Secondaries</td>
<td>$+18^\circ$, $+6^\circ$, $-6^\circ$, $-18^\circ$, $-30^\circ$</td>
</tr>
<tr>
<td>Secondary Windings Order on Limbs</td>
<td>A1 to A5, B1 to B5, C5 to C1</td>
</tr>
</tbody>
</table>

Fig. 2. Commercial 1 MVA, 6 kV phase-shifting multiwinding transformer
current, and the resulting power load profiles for the emulator and individual cells. The phase-shifted Pulse-Width Modulation (PWM) evenly distributes the power among the cells of an output phase cascade. High effective switching frequency of 100 kHz, small MV output filter \( f_{\text{res}} = 7.45 \text{ kHz} \) and fast control, e.g. discrete-time state-space feedback control [21] with closed-loop poles at \( \omega = 2 \pi \cdot 7 \text{ kHz} \) (see Appendix), result in a quasi step-shaped change in emulator and cell output power only limited by silicon carbide power module current ratings. To keep the cell dc link voltage within upper and lower boundaries for safe and reliable operation along with a moderate dc link capacitance requires a sufficiently high AFE control loop bandwidth. With fast AFE current transients, however, MWT parasitic properties have a significant impact on the AFE synchronization and control and must be considered.

III. PHASE-SHIFTING MULTIWINDING TRANSFORMER

Fig. 2 shows the commercial phase-shifting MWT used in this paper with its nameplate values listed in Table I. The secondary windings on the three legs of the transformer are composed of three groups A, B and C, each supplies \( N = 5 \) cells in series connection. The windings are numbered as A1 to A5, B1 to B5, and C5 to C1. Please note that the order of the C group is reversed to avoid additional dielectric insulation distance between the windings, as both B5 and C5 are connected to the neutral-point of the output stage. This reversed arrangement further adds up to the asymmetry. The nominal phase-shift between primary side and winding A\( k \) is the same as in B\( k \) and C\( k \) for winding index \( k = 1 \ldots N \).

Due to the discrete turns number, the actual voltage transfer ratios and the phase-shift angles are quantized and slightly deviate from the ideal ones given by the nominal phase-shifts \( \delta_{k,\text{nom}} = 60^\circ \cdot (N - k)/N - 30^\circ \). This is especially the case because of the smaller number of turns per coil in the extended delta windings on the LV side compared to the windings on the MV side [22], with up to \( +1.5\% \) amplitude error and \( \pm 2.2\% \) phase error for this MWT — similarly for comparable MWTs.

Besides the magnetic flux coupling through the core, the windings are also coupled by flux paths through the air. Recent literature [23] shows how a multwinding transformer can be modeled for multidomain simulation that combines electrical and magnetic circuits, where the magnetic permeance components represent the flux paths. The approach used in the model and presented in [24] uses the analogy between magnetic permeance and electric capacitance with the derivative of the magnetic flux as the flow variable [25] and magneto-motive-force (MMF) as the effort (or drop) variable. The magnetic energy in the model is stored in the magnetic paths through the air and the core.

The model structure is depicted in Fig. 5. It shows the wye-connected primary winding, some of the extended delta windings and one ordinary delta winding. In the model, the winding resistances are distributed on per-turn basis and not shown in the figure. In addition to the permeances \( P_c \) of the core sections, it shows the stray flux path permeances through the air \( P_{\text{air}} \). The permeances of the core sections can be calculated from core geometry and material properties.

Only very few experimental tests are needed to parametrize the magnetic permeances of the air paths, thanks to the symmetries and repetitive structures of the transformer [23]. This magnetic permeance network is interfaced by all electric terminals and effectively reflects their self and mutual coupling.

In [26] this method has successfully been applied to the medium-voltage phase-shifting MWT and experimental verification under load have confirmed the high fidelity of the model of the transformer that is shown in Fig. 2. The geometrical arrangement of the windings along the core leads to unbalanced stray fluxes, and thus result in unbalanced equivalent leakage inductances. Such effect is not present in models consisting of an ideal transformer and uncoupled, ideally balanced stray inductances, thus the ideal models are suitable for single port transformers but not MV MWTs, where the stray flux paths are more pronounced due to insulation requirements.

Measurement results of the considered MWT are plotted in Fig. 6, published in [26], and show that the stray inductance of the secondary windings significantly depends on its position on the limb. This leads to the question whether during fast power transients the grid synchronization and AFE control are robust enough to work with this variation of the stray inductance value using the same set of control and PLL parameters for all cells as it is desired in a modular design, without knowledge of the couplings and the actual phase-shift and voltage transfer ratio of each winding. Next sections address this question.
be implemented locally in the cell reducing the communication to the central application controller to a minimum. In low-dynamics applications this scheme can be a feasible solution. However, in high-dynamics applications, as it is a grid emulator, the feedback caused by the transformer impedance can significantly disturb the PLL and thereby the AFE controllers. Additionally, due to the voltage drop across the transformer impedance, the PLL can pick up the harmonics of the AFE current and reintroduce them in the current control loop causing amplification. Furthermore, with this scheme the displacement power factor at grid emulator supply terminals varies under load, and has to be compensated. Finally, the 15 three-phase filters rated for 67 kVA each are costly and bulky. Removing them would thus be advantageous and motivates the analysis of the following filter-less approach and a direct comparison of the performance of the two methods in an application where stray and mutual inductances of the MWT cause a significant feedback and interference during fast power transients.

C. No AFE Filters and a Single Primary Side PLL

If the cell input filters are omitted, only voltages of the transformer primary side can be used as PLL input. As shown in Fig. 8b the secondary side phase angles and voltage amplitudes must then be calculated from the transformer primary side PLL outputs. In this paper, transformer nameplate values are used for PLL signal processing. This way, also the possibility to avoid the transformer characterization that requires numerous measurements is considered. The nominal values naturally deviate from the actual phase-shifting angle and turn ratio of each winding of the manufactured MWT.

Regarding the system implementation, different signal processing structures are possible with PLL output being commu-
nicated to the cells or cell currents and voltages transmitted to a central controller.

With this scheme, unity power factor can be easily achieved. Regarding the quality of the sensed voltage this structure gives significant advantages as I) the supply grid has a much lower impedance, II) switching frequency harmonics are negligible as they can be mitigated by interleaving the AFE pulswidth modulation carriers, and III) a high number of current harmonics are canceled by the phase-shifting nature of the transformer. Thus, the PLL must practically only reject disturbances originating from the supply grid that are uncorrelated with AFE operation. This way the positive feedback effects are practically avoided compared to the first synchronization method.

Similarly to [28] transformer primary side PLL outputs, i.e. voltage amplitude and phase angle, are approximated to a value of secondary side voltages at no-load condition by multiplying the voltage transfer ratio respectively adding the nominal phase-shifts given on the nameplate of the transformer. In this paper, however, the transformer exhibits phase-shifts and voltage transfer ratios that additionally slightly diverge from nominal values from cell to cell. Thus, the control scheme must not only work with I) strongly varying stray inductances but also II) with errors in phase and voltage amplitude due to the mismatch between real transformer and nameplate data used for the calculations.

Furthermore, in contrast to the drive application in [28], asymmetric grid emulator output operating points need to be taken into consideration, e.g. a severe voltage sag in one of the output phases means reduced power flow in that cell group. Consequently, in contrast to [28] cell input currents need to be sinusoidal, as no mutual harmonic compensation can take place in the transformer. Sinusoidal currents however require a low dc link voltage controller bandwidth. A control scheme that allows to increase the control bandwidth while keeping the AFE currents sinusoidal is shown in the next section.

Please note that the second synchronization scheme is also an option when input filters are used, but this combination would give no advantage in costs and size of the grid emulator.

D. Simulation Results without Load

Some transformer asymmetries as well as deviations to the nameplate winding data can already be seen at no-load operation. Fig. 9 shows the simulation results at no-load condition, without switching AFEs and therefore no band-pass filters. The effect of the quantized winding turns can be easily seen in Fig. 9a: averaged over one period, amplitude output of both methods differ by less than 1.6 %, phase angles deviate from ideal ones by up to 0.3° in either directions, i.e. as expected.

PLL outputs additionally unveil the effect of the magnetic asymmetry of the planar core transformer resulting in a small second grid frequency harmonic in amplitude and phase. As shown in Fig. 9b, this distortion is clearly related to the position of a winding on the limbs, not to the extended delta turn ratio of the windings. The outer windings that are closer to the yokes are more affected than the innermost ones. This magnetic non-ideality of a finite-length transformer limbs can significantly affect the operation under load. The average error is linked to the discrete number of winding turns.

V. GRID EMULATOR AFE PERFORMANCE UNDER LOAD

The 15 power cells of the grid emulator are rated for a total power of 1 MVA, their parameters are summarized in Table II. For the PLL investigation the switching frequency effects of the CHB output stage can be neglected, so the cell dc links can be loaded with corresponding fundamental frequency currents to reduce the simulation time. As shown in Section II, the dc link voltage control is disturbed by the cell's output current and the most challenging disturbance is a power step in the cell output.

The AFE input currents are controlled to be sinusoidal using Proportional-Resonant (PR) controllers in stationary reference frame (αβ coordinates) while the the dc link voltage is controlled with a Proportional-Integral (PI) controller and instantaneous power equations [29], [30] as shown in Fig. 10. The sampled dc link voltage $v_{dc}$ is notched at double CHB output voltage frequency and an active damping is added for operation without input filter.

The PLL and controller parameters listed in Table III are same for all cells, despite having different stray inductances in the plant. For the primary side based synchronization scheme that does not require an input filter inductor, current and
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TABLE II
REGENERATIVE CELL PARAMETERS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Apparent Power Rating</td>
<td>67 kVA</td>
</tr>
<tr>
<td>AFE Nominal Current</td>
<td>57 A</td>
</tr>
<tr>
<td>Inverter HB Nominal Current</td>
<td>96 A</td>
</tr>
<tr>
<td>Nominal DC Link Voltage</td>
<td>1100 V</td>
</tr>
<tr>
<td>DC link Capacitance</td>
<td>4.2 mF</td>
</tr>
<tr>
<td>Input Filter Inductance</td>
<td>3.4 mH</td>
</tr>
<tr>
<td>Input Filter Inductor Resistance</td>
<td>10 mΩ</td>
</tr>
</tbody>
</table>
| AFE Sampling and Switching Frequency | 10 kHz | Triangle Carrier PWM
| AFE Zero-Sequence Voltage Injection | min/max |

At $t = 0.02\text{s}$, the CHB stage is loaded with symmetrical three-phase currents, AFE controllers and switching are enabled and have to stabilize the dc link voltage using AFE currents.

At $t = 0.12\text{s}$, the CHB stage generates another power step. To demonstrate the controller performance and reserves, the load power is reversed.

Fig. 11 shows the response of the two cases with the grid side values first, followed by cell input currents, then dc link voltages, and finally summarized by the input and output power balance.

In response to the first power step in the output H-bridges from zero to 1 MW in total, cell dc link voltages deviate from their nominal value and exhibit a second harmonic of the output power pulsation as shown in the dc link voltage subplots. On request of the cell voltage controllers, the inner current control loop of each cell ramps up AFE currents to bring the average cell voltage back to nominal and establish an input and output power balance as shown in the subplots.

The 45 cell input currents are aligned to the PLL output voltages, with every three currents (e.g. phase R of the cells A1, B1, and C1) having a similar phase angle and amplitude in a balanced steady state. Then, only 15 currents are distinguishable in the plot. All secondary side currents are phase-shifted by the transformer winding structure and their sum appears on its primary side (first subplot).

Fig. 12 shows the outputs of the transformer primary side voltage based PLL (in black) and those using the secondary side terminal voltages as inputs (colored) under load. The first two subplots show the estimated phase angles and voltage amplitudes. Knowing the exact grid voltage phase angle, the difference between the PLL estimated phase angle and grid phase is plotted in the third subplot. Here, one can see, on time average, the secondary side voltage phase angles leading before their ideal value during rectification and lagging during inversion. Similarly, the estimated secondary side amplitude is lower than its no-load value during rectification and higher during inversion. Both effects are due to the voltage drop across the transformer impedance and can lead to a positive feedback effect, since for a constant power setpoint and a lower voltage the current will increase, causing further voltage drop.

To show the effect of the omitted filters on current quality, Fig. 13 shows the current harmonics spectrum on the transformer primary side, and input currents of the cells A1 to A5.

B. Discussion

According to Fig. 11, the filter-less solution performs well despite transformer non-idealities, and both configurations exhibit well-shaped steady-state waveforms: The supply grid currents are sinusoidal, dc link voltages are well-balanced, and the AFE currents have minimal distortion. The latter will allow to operate the grid emulator with harmonics and power asymmetries at the CHB output. The main difference of steady-state is that the primary side aligned scheme inherently features unity power factor, i.e. does not require further compensation.

Regarding the transient behavior, which is of utmost importance for high-dynamic grid emulator operation, the filter-less
Fig. 11. Simulation results for ±1 MW steady-state and transient operation: (a) using transformer secondary side PLLs and cell input filters, and (b) using transformer primary side PLL, no cell input filters. At \( t = 0.02 \) s, the emulator output power is stepped up by 1 MW and the AFE control has to compensate the sag in the dc link voltages; at \( t = 0.12 \) s, an ideal power reversal causes a step of −2 MW in the emulator output power and the AFE control has to compensate the swell in the dc link voltages. Case (b) features faster transient response and dc link voltage regulation.

solution clearly outperforms the one with filter and secondary side synchronization. The AFE currents are ramped up and reversed within about one third of the grid period, compared to a full grid period with filter. The disturbance rejection of the dc link control is improved with a higher bandwidth and increased loop gain: sags and swells of the dc link voltage are smaller and steady-state is reached within few grid cycles, in contrast to the filter case where the steady state is not reached within simulated time.

The reasons for different control dynamics are:

(I) As shown in Fig. 12, secondary side PLLs are strongly disturbed during transients. Hereby, the closer a winding is located to the yoke, the more it is affected by oscillations. This effect is not present if a transformer model with uncoupled equal secondary stray inductances is used. The disturbance increases with processed power as the leakage flux among the windings increases. To regain stability when using the detailed permeance-based transformer model, the controller phase margin was increased and lead to a lower control loop bandwidth.

(II) With the proportional gain of the current controller kept almost constant and filter inductor removed, current control bandwidth of the filter-less solution increased by four to five times. In cascaded control, this consequently allowed to increase the dc link controller bandwidth by three times, reaching the current limit that protects the semiconductors.

(III) Additionally, the use of the primary side PLL outputs, that is not affected by the power transients, for the current and voltage controllers increased the robustness during these transients.

Furthermore, in the filter-less case, the analysis of the harmonic spectrum in Fig. 13a confirms the sinusoidal waveform of the transformer primary side current.
PLL Output: Phase Angles
PLL Output: Amplitudes
Difference between PLL Phase Angles and Grid Phase Angle

Time (s)
0.00 0.02 0.04 0.06 0.08 0.10 0.12 0.14 0.16 0.18 0.20 0.22
(°)
-40 -20 0 20 40
C1 C1 A1 A1

Fig. 12. Simulation results for ±1 MW steady-state and transient operation shown in Fig. 11: transformer primary side and transformer secondary side PLL outputs. Primary side based PLL have steady outputs (black curves), while outputs of secondary side PLLs (colored curves) depend on the power flow and feature significant disturbances. While the PLL works relatively good for innermost secondary winding (B3), outer windings with higher stray inductance are involved in current oscillations among each other induced by the power transients. The voltage drop of these oscillations is picked up by the PLLs and compromises the reliability of this synchronization scheme. PLL output of the innermost (B3) and outermost windings (A1 and C1) are highlighted.

Fig. 13. (a) Grid emulator input current harmonic spectrum for the period \( t =0.10 \) s to 0.12 s of Fig. 11b easily fulfills IEEE 519 current harmonics limits, THD including switching harmonics is 2.1 %. Reduced fundamental and presence of a dc component are due to the unfinished transient. (b) Cell input currents in the same period exhibit low switching current ripple also without filter inductor.

All in all, the simulation results obtained using a detailed magnetic model of a phase-shifting multiwinding transformer show, that omitting the bulky AFE input filters and changing the synchronization scheme from multiple measurements on the low-voltage secondary side terminals to a single measurement on the medium-voltage side result in a more compact and more robust cell supply for a high-dynamic multicell topology based grid emulator.

**Conclusion**

The paper demonstrates that primary side voltage measurements and nominal nameplate data are sufficient for effective synchronization and operation of the AFEs despite non-ideal turn ratios, non-ideal phase-shift angles and highly unequal distribution of stray inductances of the commercial phase-shifting multiwinding transformer. Omitting the filter components at cell inputs and using the stray inductance of the transformer resulted not only in a cheaper and more compact grid emulator design, additionally, key performance indices like robust and fast transient response to load variations have been further improved which is crucial for a high-performance grid emulator.

Further research will cover practical implementation and experiment of the synchronization scheme with the 1 MVA transformer and high bandwidth control methods to deal with the unequal stray inductance and inter-winding couplings.
Fig. 14 shows the plant and closed-loop transfer functions of the grid emulator output voltage control that uses full state feedback for pole placement.

REFERENCE


[2] -


Min Luo (M’13) was born in Beijing, China, in 1986. He received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 2009, M.S. degree in electrical power engineering from RWTH Aachen University, Aachen, Germany, in 2012, and PhD degree in electrical engineering from Swiss Institute of Technology Lausanne (EPFL), Switzerland, in 2018. Since 2012 he has been with Plexim as application engineer, working on the toolchain PLECS for fast simulation of power electronic systems. His current research interest include dynamic modelling of magnetic components and real-time HIL simulation of power converters.

Drazen Dujic (S’03–M’09–SM’12) received the Dipl.-Ing. and M.Sc. degrees from the University of Novi Sad, Novi Sad, Serbia, in 2002 and 2005, respectively, and the Ph.D. degree from Liverpool John Moores University, Liverpool, U.K., in 2008, all in electrical engineering. From 2002 to 2006, he was a Research Assistant with the Department of Electrical Engineering, University of Novi Sad. From 2006 to 2009, he was a Research Associate with Liverpool John Moores University. From 2009 to 2013, he was with the ABB Corporate Research Center, Baden, Switzerland, as a Principal Scientist working on Power Electronics Projects. During 2010–2011, he was involved in the development of the Power Electronic Traction Transformer. From 2013 to 2014, he was with ABB Medium Voltage Drives, Turgi, Switzerland, as an R&D Platform Manager. He is currently an Assistant Professor with the Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, where he is also the Director of the Power Electronics Laboratory. He has authored/coauthored more than 120 scientific publications and has filed 14 patents. His current research interests include the areas of design and control of advanced high-power electronics systems and high-performance drives. Dr. Dujic is an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEETRANSACTIONS ON POWER ELECTRONICS, and IET Electric Power Applications. In 2018 he received EPE Outstanding Service Award and in 2014, he received the Isao Takahashi Power Electronics Award for outstanding achievement in power electronics.