Pushing the Limits of Efficiency and Power Density in High-Frequency Power Conversion Based on Wide-Band-Gap Technologies

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par
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Acceptée sur proposition du jury
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Love is a teacher, but one must know how to acquire it, for it is difficult to acquire, it is dearly bought, by long work over a long time, for one ought to love not for a chance moment but for all time…

— Fyodor Dostoevsky, The Brothers Karamazov

To my family, and to my teachers…
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I express my highest gratitude to my beloved parents, whose continuous support, guidance and sacrifice have been a catalyst for my success. You were right there beside me, paying careful attention and aiding me with important decisions in my life. The same is true of Aryan, my always reliable and adventurous brother. Last, but not least, I thank all my teachers whose presence brought out the best in me.

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Armin Jafari
Abstract

The emergence of wide-band-gap (WBG) power transistors with low conduction losses and high-speed switching speeds has paved the way for more-than-ever efficient power electronics systems and huge energy saving potentials. Likewise, power density- the ratio of power to volume (or weight)-can be significantly increased in power converters based on gallium nitride (GaN) and silicon carbide (SiC) transistors. Converters with high efficiencies and large power densities are essential to forthcoming applications such as electric aircrafts, hyperloop transportation systems and direct-current (DC) grids. Nonetheless, major barriers for realizing such converters are:

- Lack of important information in datasheets and models from WBG device manufacturers, and huge diversities in the performance of WBG transistors based on different GaN and SiC technologies.

- Shortcomings of existing tools for accurate system-level and component-level performance analysis and loss measurement in efficient power converters at high-frequency (HF) and very-high-frequency (VHF) domains.

- Necessity to enhance traditional converter topologies for compatibility with WBG devices, by designing high-quality magnetics and implementing novel control strategies to maximize their efficiency and power density, which are typically two opposing objectives.

Thesis in Chapter 2 focuses on accurate methods for voltage and current rise rate measurements of high-speed GaN and SiC transistors for pulsed-power applications, highlighting the effect of different parameters on the device switching speed. Next, we propose measurement methods for evaluation of gate loss, conduction and dynamic ON-resistance degradation loss and output capacitance loss in soft-switched WBG transistors for frequencies of up to 40 MHz, providing an insightful performance comparison between various SiC and GaN technologies for HF and VHF resonant and quasi-resonant power converters.

High-quality magnetic components, namely inductors and transformers, are inseparable building blocks of efficient power converters. Chapter 3 is dedicated to characterizing magnetics in the HF domain, with an overview of different loss evaluation methods.

Chapter 4 proposes advanced calorimetric techniques: First, a novel dual-chamber calorimeter with an unprecedented measurement accuracy and range is proposed for sensitive loss measurements in power electronics building blocks (e.g., HF inductors and transformers) and efficiency evaluations in highly-efficient converters where electrical measurements are prone to large errors. Next, a thermal method based on temperature mapping is presented, suitable for assessment of losses and their distribution in HF and
Abstract

VHF power circuits.

Improved DC-DC topologies for efficient operation at HF are the subjects of Chapter 5. An enhanced dual-active-bridge (E-DAB) topology is proposed for efficiency preservation over wide voltage gains, achieving a peak efficiency of 97.4% and a power density of 10 kW/l. By applying a new operation mode based on impulse rectification, traditional boost converters can achieve zero-voltage switching. Thanks to several optimizations in magnetics design, device selection, layout and control, a converter with an outstanding peak efficiency of 98.6% and a power density of 52 kW/l is realized.

The thesis provides insights for power electronics designers and device engineers to push the limits of conversion efficiency and power density to the maximum using WBG technologies.

Key words: Efficiency, power density, wide-band-gap, high-frequency magnetics, advanced measurements, calorimetric techniques, enhanced DAB, soft-switching boost converter, GaN, SiC
Zusammenfassung

Das Aufkommen von Leistungstransistoren mit breite Bandlücke (WBG) mit geringen Leitungsverlusten und hohen Schaltgeschwindigkeiten hat den Weg für immer effizientere Leistungselektroniksysteme und enorme Energieeinsparpotenziale geebnet. Ebenso kann die Leistungsdichte - das Verhältnis von Leistung zu Volumen (oder Gewicht) - in Leistungswandlern auf der Basis von Galliumnitrid- (GaN) und Siliziumkarbid- (SiC) -Transistoren signifikant erhöht werden. Konverter mit hohen Wirkungsgraden und großen Leistungsdichten sind für bevorstehende Anwendungen wie Elektroflugzeuge, Hyperloop-Transportsysteme und Gleichstromnetze von wesentlicher Bedeutung. Die größten Hindernisse für die Realisierung solcher Konverter sind jedoch:

- Mangel an wichtigen Informationen in Datenblättern und Modellen von WBG-Gerateherstellern und große Unterschiede in der Leistung von WBG-Transistoren, die auf verschiedenen GaN- und SiC-Technologien basieren.
- Mängel vorhandener Tools für eine genaue Leistungsanalyse auf Systemebene und Komponentenebene sowie für die Verlustmessung in effizienten Stromrichtern in Hochfrequenz (HF) und sehr Hochfrequenz (VHF) Domänen.
- Notwendigkeit, herkömmliche Konverterzopologien für die Kompatibilität mit WBG-Geräten zu verbessern, indem hochwertige Induktivitäten und Transformatoren entworfen und neuartige Steuerungsstrategien implementiert werden, um deren Effizienz und Leistungsdichte zu maximieren, die normalerweise zwei gegensätzliche Ziele sind.


Die Arbeit bietet Einblicke für Leistungselektronikdesigner und Geräteingenieure, mithilfe von WBG-Technologien die Grenzen der Umwandlungseffizienz und Leistungsdichte maximal zu überschreiten.
Résumé

L’émergence de transistors de puissance à large bande interdite (WBG) avec de faibles pertes de conduction et des vitesses de commutation rapides a ouvert la voie à des systèmes électroniques de puissance plus efficaces que jamais et à d’énormes potentiels d’économie d’énergie. De même, la densité de puissance - le rapport puissance/volume (ou poids) - peut être considérablement augmentée dans les convertisseurs de puissance basés sur des transistors en nitrure de gallium (GaN) et en carbure de silicium (SiC). Les convertisseurs avec des rendements élevés et de grandes densités de puissance sont essentiels pour les applications à venir telles que les avions électriques, les systèmes de transport hyperloop et les réseaux de courant continu (DC). Néanmoins, les principaux obstacles à la réalisation de tels convertisseurs sont :

• Manque d’informations importantes dans les fiches techniques et les modèles des fabricants d’appareils WBG, et grande diversité dans les performances des transistors WBG basés sur différentes technologies GaN et SiC.

• Les lacunes des outils existants pour l’analyse précise des performances au niveau du système et des composants et la mesure des pertes dans les convertisseurs de puissance efficaces dans les domaines haute fréquence (HF) et très haute fréquence (VHF).

• Nécessité d’améliorer les topologies de convertisseur traditionnelles pour la compatibilité avec les appareils WBG, en concevant des magnétiques de haute qualité et en mettant en œuvre de nouvelles stratégies de contrôle pour maximiser leur efficacité et leur densité de puissance, qui sont généralement deux objectifs opposés.

La thèse du chapitre 2 se concentre sur des méthodes précises pour les mesures de taux de montée en tension / courant des transistors GaN et SiC à grande vitesse pour les applications à puissance pulsée, mettant en évidence l’effet de différents paramètres sur la vitesse de commutation de l’appareil. Ensuite, nous proposons des méthodes de mesure pour l’évaluation de la perte d’entrée, de la conduction et de la dégradation de la résistance dynamique ON et de la perte de capacité de sortie dans les transistors WBG à commutation douce pour des fréquences allant jusqu’à 40 MHz, offrant une comparaison des performances perspicace entre diverses technologies SiC et GaN dans Convertisseurs de puissance résonants et quasi-résonnants HF et VHF.

Les composants magnétiques de haute qualité, à savoir les inducteurs et les transformateurs, sont des éléments constitutifs indissociables de convertisseurs de puissance efficaces. Le chapitre 3 est dédié à la caractérisation du magnétisme dans le domaine HF, avec un aperçu des différentes méthodes d’évaluation des pertes.
Résumé

Le chapitre 4 propose des techniques calorimétriques avancées : Premièrement, un nouveau calorimètre à double chambre avec une précision et une plage de mesure sans précédent est proposé pour les mesures de pertes sensibles dans les blocs de construction de l’électronique de puissance (par exemple, les inducteurs et les transformateurs HF) et les évaluations d’efficacité dans les convertisseurs hautement efficaces où les mesures électriques sont sujettes à de grosses erreurs. Ensuite, une méthode thermique basée sur la cartographie des températures est présentée, adaptée à l’évaluation des pertes et de leur distribution dans les circuits de puissance HF et VHF.

Les topologies DC-DC améliorées pour un fonctionnement efficace en HF sont les sujets du chapitre 5. Une topologie améliorée à Dual-Active-Bridge (E-DAB) est proposée pour la préservation de l’efficacité sur de larges gains de tension, atteignant un rendement de crête de 97,4% et une puissance densité de 10 kW/l. En appliquant un nouveau mode de fonctionnement basé sur le redressement des impulsions, les convertisseurs boost traditionnels peuvent réaliser une commutation à tension nulle. Grâce à plusieurs optimisations dans la conception magnétique, la sélection des appareils, la disposition et le contrôle, un convertisseur avec un rendement de crête exceptionnel de 98,6% et une densité de puissance de 52 kW/l est réalisé.

La thèse fournit des informations aux concepteurs d’électronique de puissance et aux ingénieurs de dispositifs pour repousser au maximum les limites de l’efficacité de conversion et de la densité de puissance en utilisant les technologies WBG.
# Symbols and Acronyms

## Symbols

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Definition</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$B$</td>
<td>Magnetic flux density</td>
<td>T</td>
</tr>
<tr>
<td>BFOM</td>
<td>Baliga’s figure of merit</td>
<td>W/m²</td>
</tr>
<tr>
<td>$B_S$</td>
<td>Saturation magnetic flux density</td>
<td>T</td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth</td>
<td>Hz</td>
</tr>
<tr>
<td>$C_{CH}$</td>
<td>Charging capacitor</td>
<td>F</td>
</tr>
<tr>
<td>$C_{DS}$</td>
<td>Drain-to-source capacitance</td>
<td>F</td>
</tr>
<tr>
<td>$C_{GD}$</td>
<td>Gate-to-drain capacitance</td>
<td>F</td>
</tr>
<tr>
<td>$C_{GS}$</td>
<td>Gate-to-source capacitance</td>
<td>F</td>
</tr>
<tr>
<td>$C_{ISS}$</td>
<td>Input capacitance</td>
<td>F</td>
</tr>
<tr>
<td>$C_{OSS}$</td>
<td>Output capacitance</td>
<td>F</td>
</tr>
<tr>
<td>$C_{OSS}^e$</td>
<td>Energy-related output capacitance</td>
<td>F</td>
</tr>
<tr>
<td>$c_p$</td>
<td>Isobaric specific heat capacity of coolant</td>
<td>J/kg·K</td>
</tr>
<tr>
<td>$C_{PRIM}$</td>
<td>Equivalent primary bridge capacitance</td>
<td>F</td>
</tr>
<tr>
<td>$C_{REF}$</td>
<td>Reference capacitor</td>
<td>F</td>
</tr>
<tr>
<td>CRR</td>
<td>Current rise rate</td>
<td>A/s</td>
</tr>
<tr>
<td>$C_{SECON}$</td>
<td>Equivalent secondary bridge capacitance</td>
<td>F</td>
</tr>
<tr>
<td>$D$</td>
<td>Duty cycle</td>
<td></td>
</tr>
<tr>
<td>$E_{DISS}$</td>
<td>Energy dissipated in each charging/discharging of $C_{OSS}$</td>
<td>J</td>
</tr>
<tr>
<td>$e_I$</td>
<td>DC current measurement error</td>
<td>A</td>
</tr>
<tr>
<td>$e_T$</td>
<td>Temperature measurement error</td>
<td>K</td>
</tr>
<tr>
<td>$e_V$</td>
<td>DC voltage measurement error</td>
<td>V</td>
</tr>
<tr>
<td>$\eta$</td>
<td>Conversion efficiency</td>
<td></td>
</tr>
<tr>
<td>$f$</td>
<td>Operating frequency</td>
<td>Hz</td>
</tr>
<tr>
<td>$f_H$</td>
<td>Upper operating frequency</td>
<td>Hz</td>
</tr>
<tr>
<td>$f_{SW}$</td>
<td>Switching frequency</td>
<td>Hz</td>
</tr>
<tr>
<td>$f_{OSC}$</td>
<td>Oscillation frequency</td>
<td>Hz</td>
</tr>
<tr>
<td>$\phi$</td>
<td>Phase shift</td>
<td>°</td>
</tr>
<tr>
<td>$G$</td>
<td>Voltage gain</td>
<td></td>
</tr>
<tr>
<td>$H_C$</td>
<td>Magnetic coercivity</td>
<td>A/m</td>
</tr>
<tr>
<td>$i_{DS}$</td>
<td>Drain-to-source current</td>
<td>A</td>
</tr>
<tr>
<td>$I_{PRIM}$</td>
<td>Primary-side transformer current</td>
<td>A</td>
</tr>
<tr>
<td>$I_{SECON}$</td>
<td>Secondary-side transformer current</td>
<td>A</td>
</tr>
<tr>
<td>$J$</td>
<td>Current density</td>
<td>A/m²</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Unit</td>
</tr>
<tr>
<td>--------</td>
<td>-----------------------------------------------------------------------------</td>
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</tr>
<tr>
<td>JFOM</td>
<td>Johnson’s figure of merit</td>
<td>Hz·V</td>
</tr>
<tr>
<td>KFOM</td>
<td>Figure of merit for high-frequency magnetic materials</td>
<td>T·Ω·m²/J</td>
</tr>
<tr>
<td>k₁</td>
<td>Integral coefficient</td>
<td></td>
</tr>
<tr>
<td>kₚ</td>
<td>Proportional coefficient</td>
<td></td>
</tr>
<tr>
<td>kₜ</td>
<td>Thermal conductivity</td>
<td>W/m·K</td>
</tr>
<tr>
<td>Lₚₐᵦ</td>
<td>Parasitic inductance</td>
<td>H</td>
</tr>
<tr>
<td>Lₜ</td>
<td>Leakage inductance</td>
<td>H</td>
</tr>
<tr>
<td>µᵣ</td>
<td>Relative magnetic permeability</td>
<td>H/m</td>
</tr>
<tr>
<td>n</td>
<td>Transformer turns ratio (secondary to primary)</td>
<td></td>
</tr>
<tr>
<td>P_CAL</td>
<td>Power dissipation in calibrator chamber</td>
<td>W</td>
</tr>
<tr>
<td>P_CON</td>
<td>Transistor conduction loss</td>
<td>W</td>
</tr>
<tr>
<td>P_DUT</td>
<td>Power dissipation in test chamber</td>
<td>W</td>
</tr>
<tr>
<td>P_DYN</td>
<td>Transistor loss due to dynamic ON-resistance degradation</td>
<td>W</td>
</tr>
<tr>
<td>P_FAN</td>
<td>Power dissipation in calorimeter inner fans</td>
<td>W</td>
</tr>
<tr>
<td>P_G</td>
<td>Gate loss</td>
<td>W</td>
</tr>
<tr>
<td>P_GD</td>
<td>Gate driver loss</td>
<td>W</td>
</tr>
<tr>
<td>P_IN</td>
<td>Input power</td>
<td>W</td>
</tr>
<tr>
<td>P_LOSS</td>
<td>Actual power dissipation</td>
<td>W</td>
</tr>
<tr>
<td>P_O</td>
<td>Output capacitance loss</td>
<td>W</td>
</tr>
<tr>
<td>P_OUT</td>
<td>Output power</td>
<td>W</td>
</tr>
<tr>
<td>P_TR</td>
<td>Transistor loss</td>
<td>W</td>
</tr>
<tr>
<td>P_V</td>
<td>Magnetic hysteresis and eddy-current losses per unit of volume</td>
<td>W/m³</td>
</tr>
<tr>
<td>q</td>
<td>Electric charge</td>
<td>C</td>
</tr>
<tr>
<td>Q</td>
<td>Quality factor</td>
<td></td>
</tr>
<tr>
<td>Q_G</td>
<td>Transistor gate charge</td>
<td>C</td>
</tr>
<tr>
<td>ρ</td>
<td>Coolant volumetric density</td>
<td>kg/m³</td>
</tr>
<tr>
<td>ρ_c</td>
<td>Electrical resistivity</td>
<td>Ω·m</td>
</tr>
<tr>
<td>R_AC</td>
<td>Alternating current resistance</td>
<td>Ω</td>
</tr>
<tr>
<td>R_C</td>
<td>Core-loss equivalent series resistance</td>
<td>Ω</td>
</tr>
<tr>
<td>R_CH</td>
<td>Charging resistor</td>
<td>Ω</td>
</tr>
<tr>
<td>R_COND</td>
<td>Conductive resistance</td>
<td>Ω</td>
</tr>
<tr>
<td>R_DS(ON)</td>
<td>Transistor ON-state resistance</td>
<td>Ω</td>
</tr>
<tr>
<td>R_LOAD</td>
<td>Load resistance</td>
<td>Ω</td>
</tr>
<tr>
<td>R_OFF</td>
<td>Gate drive turn-OFF resistance</td>
<td>Ω</td>
</tr>
<tr>
<td>R_ON</td>
<td>Gate drive turn-ON resistance</td>
<td>Ω</td>
</tr>
<tr>
<td>R_Prox</td>
<td>Proximity-effect resistance</td>
<td>Ω</td>
</tr>
<tr>
<td>T_amb</td>
<td>Ambient temperature</td>
<td>°C</td>
</tr>
<tr>
<td>T_CASE</td>
<td>Case temperature (e.g. of a transistor)</td>
<td>°C</td>
</tr>
<tr>
<td>T_GD</td>
<td>Gate driver temperature</td>
<td>°C</td>
</tr>
<tr>
<td>T_TR</td>
<td>Transistor temperature</td>
<td>°C</td>
</tr>
<tr>
<td>T_HS</td>
<td>Hot-spot temperature</td>
<td>°C</td>
</tr>
<tr>
<td>V_BR</td>
<td>Breakdown voltage</td>
<td>V</td>
</tr>
<tr>
<td>V_DC</td>
<td>DC-link voltage</td>
<td>V</td>
</tr>
<tr>
<td>V_DS</td>
<td>Drain-to-source voltage</td>
<td>V</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Unit</td>
</tr>
<tr>
<td>---------</td>
<td>-----------------------------------------------------------</td>
<td>------</td>
</tr>
<tr>
<td>$v_{GS}$</td>
<td>Gate-to-source voltage</td>
<td>V</td>
</tr>
<tr>
<td>$v_{IN}$</td>
<td>Input voltage</td>
<td>V</td>
</tr>
<tr>
<td>$v_{LOAD}$</td>
<td>Load voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OFF}$</td>
<td>Turn-OFF voltage for gate</td>
<td>V</td>
</tr>
<tr>
<td>$V_{ON}$</td>
<td>Turn-ON voltage for gate</td>
<td>V</td>
</tr>
<tr>
<td>$v_{OUT}$</td>
<td>Output voltage</td>
<td>V</td>
</tr>
<tr>
<td>$v_{PRIMARY}$</td>
<td>Transformer primary-side voltage</td>
<td>V</td>
</tr>
<tr>
<td>VRR</td>
<td>Voltage rise rate</td>
<td>V/s</td>
</tr>
<tr>
<td>$v_{SECONDARY}$</td>
<td>Transformer secondary-side voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_{TH}$</td>
<td>Threshold voltage (for transistor turn ON)</td>
<td>V</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Full name</td>
<td></td>
</tr>
<tr>
<td>--------------</td>
<td>-----------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>AC</td>
<td>Alternating Current</td>
<td></td>
</tr>
<tr>
<td>AWG</td>
<td>American Wire Gauge</td>
<td></td>
</tr>
<tr>
<td>CAL</td>
<td>Calibration/Calibrator</td>
<td></td>
</tr>
<tr>
<td>CC</td>
<td>Constant Current</td>
<td></td>
</tr>
<tr>
<td>CCM</td>
<td>Continuous Conduction Mode</td>
<td></td>
</tr>
<tr>
<td>CV</td>
<td>Constant Voltage</td>
<td></td>
</tr>
<tr>
<td>DAB</td>
<td>Dual Active Bridge</td>
<td></td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
<td></td>
</tr>
<tr>
<td>DCM</td>
<td>Discontinuous Conduction Mode</td>
<td></td>
</tr>
<tr>
<td>DMM</td>
<td>Digital Multi Meter</td>
<td></td>
</tr>
<tr>
<td>DPT</td>
<td>Double-Pulse Test</td>
<td></td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processor</td>
<td></td>
</tr>
<tr>
<td>DUT</td>
<td>Device Under Test</td>
<td></td>
</tr>
<tr>
<td>E-DAB</td>
<td>Enhanced Dual Active Bridge</td>
<td></td>
</tr>
<tr>
<td>EM</td>
<td>Electromagnetic</td>
<td></td>
</tr>
<tr>
<td>EMI</td>
<td>Electromagnetic Interference</td>
<td></td>
</tr>
<tr>
<td>EV</td>
<td>Electric Vehicle</td>
<td></td>
</tr>
<tr>
<td>FEA</td>
<td>Finite-Element Analysis</td>
<td></td>
</tr>
<tr>
<td>FET</td>
<td>Field-Effect Transistor</td>
<td></td>
</tr>
<tr>
<td>FOM</td>
<td>Figure of Merit</td>
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<tr>
<td>GaN</td>
<td>Gallium Nitride</td>
<td></td>
</tr>
<tr>
<td>GIT</td>
<td>Gate-Injection Transistor</td>
<td></td>
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<tr>
<td>GND</td>
<td>Ground</td>
<td></td>
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<tr>
<td>HF</td>
<td>High Frequency</td>
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</tr>
<tr>
<td>HV</td>
<td>High Voltage</td>
<td></td>
</tr>
<tr>
<td>I2C</td>
<td>Inter-Integrated Circuit</td>
<td></td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated-Gate Bipolar Transistors</td>
<td></td>
</tr>
<tr>
<td>IMS</td>
<td>Insulated Metal Substrate</td>
<td></td>
</tr>
<tr>
<td>IR</td>
<td>Infrared</td>
<td></td>
</tr>
<tr>
<td>LED</td>
<td>Light-Emitting Diode</td>
<td></td>
</tr>
<tr>
<td>lidar</td>
<td>Light Detection And Ranging</td>
<td></td>
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<tr>
<td>LV</td>
<td>Low Voltage</td>
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<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field-Effect Transistor</td>
</tr>
<tr>
<td>MV</td>
<td>Medium Voltage</td>
</tr>
<tr>
<td>NR</td>
<td>Nonlinear Resonance</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PI</td>
<td>Proportional Integral</td>
</tr>
<tr>
<td>PSFB</td>
<td>Phase-Shifted Full-Bridge</td>
</tr>
<tr>
<td>p.u.</td>
<td>per unit</td>
</tr>
<tr>
<td>PV</td>
<td>Photovoltaic</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse-Width Modulation</td>
</tr>
<tr>
<td>Si</td>
<td>Silicon</td>
</tr>
<tr>
<td>SiC</td>
<td>Silicon Carbide</td>
</tr>
<tr>
<td>Si-SJ</td>
<td>Silicon Super Junction</td>
</tr>
<tr>
<td>SPI</td>
<td>Serial Peripheral Interface</td>
</tr>
<tr>
<td>SPS</td>
<td>Single Phase Shift</td>
</tr>
<tr>
<td>ST</td>
<td>Sawyer–Tower</td>
</tr>
<tr>
<td>UART</td>
<td>Universal Asynchronous Receiver-Transmitter</td>
</tr>
<tr>
<td>VHF</td>
<td>Very High Frequency</td>
</tr>
<tr>
<td>VTOL</td>
<td>Vertical Take-Off and Landing</td>
</tr>
<tr>
<td>WBG</td>
<td>Wide-Band-Gap</td>
</tr>
<tr>
<td>ZVS</td>
<td>Zero-Voltage Switching</td>
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1 Introduction

Global energy consumption has been continuously increasing, from a total of 106.161 PWh in 1990 to 173.34 PWh in 2019 [1]. As Figure 1.1 presents, a huge extent of the entire energy consumption comes from non-renewable resources, including fossil fuels (i.e. oil, natural gas and coal) and nuclear power. Low costs of energy generation using these resources plays a significant role in their further exploitation. However, global warming, air pollution and wastewater generation are among the unfavorable and hidden prices we pay for using them [2].

Although renewable energy resources such as solar and wind power, modern biofuels, hydropower and geothermal power produce much lower environmental pollution than the non-renewable resources, their contribution to the total energy production is orders of magnitude lower than that of the non-renewable resources, as shown in Figure 1.1.

Electricity, is one of the most versatile forms of energy, not only generated directly from renewable resources such as solar cells and wind turbines, but also converted from those that are non-renewable.

Figure 1.1 – Global primary energy consumption by source from 1990 to 2019.
Electricity generation is growing on a fast pace. Based on [3], the generation has been doubled since 1990, with the share of electricity to the total generated energy increasing by about 35%, as shown in Figure 1.2. A step towards reducing the damaging effects of massive energy generation using non-renewable resources is the increase in efficiency ($\eta$) of electrical power conversion systems. This is especially important at the consumer end as some one billion people on earth still do not have access to the electricity. Furthermore, industrial applications that require electricity such as data centers and electric transportation are increasing rapidly [4, 5].

1.1 Wide-Band-Gap Semiconductors

Power electronics is the technology responsible for the control and conversion of electric power from one form to another based on solid-state electronic devices and circuits.

In 1959, metal–oxide–semiconductor field-effect transistor (MOSFET) based on silicon (Si) was developed, which was a breakthrough in power electronics, especially after commercializing power MOSFETs in the 1970s [6, 7]. At about four decades later, field-effect transistors (FETs) based on wide-band-gap (WBG) materials, namely silicon carbide (SiC) and gallium nitride (GaN), emerged with an incredibly better performance compared to the existing Si-based devices. The band gap of a semiconductor is the minimum energy required to excite an electron that is stuck in its bound state into a free state where it can participate in conduction. Conventional semiconductors like silicon have a band gap in the range of 1 - 1.5 electronvolt (eV), whereas WBG materials have band gaps in the range of 2 - 4 eV [8].

Johnson’s figure of merit (FOM), JFOM, was first proposed by Edward O. Johnson in 1965 to compare different semiconductor materials for their high-frequency (HF) performance as power transistors [9]. Later in 1983, Baliga’s FOM (BFOM) was proposed as a measure of conduction losses for FETs based on different semiconductors [10, 11].
1.1. Wide-Band-Gap Semiconductors

Si, SiC and GaN materials are compared for their JFOM and BFOM in Figure 1.3, and the values are relative to those of Si. Both SiC and GaN exhibit one order-of-magnitude higher JFOM, which makes them suitable for HF applications that require high breakdown voltages. Furthermore, the higher BFOM for SiC and GaN transistors indicates that they can operate with lower conduction losses compared to their Si counter parts (with GaN obtaining the highest BFOM, an order-of-magnitude higher than SiC).

Today, normally-OFF GaN transistors with blocking voltages from a few tens of volts up to 900 V are commercially available at different current ratings, suitable for low-voltage (LV) applications (i.e. voltages < 1 kV). SiC transistors currently exist commercially for voltages between 650 V and 1.7 kV, with SiC MOSFETs up to 15 kV being already demonstrated in medium-voltage (MV) applications by several research groups [4, 12, 13].

Over the past few years, industry has started a migration towards power electronics systems based on WBG transistors, and the market for these transistors and converters which employ them is growing rapidly [14, 15]. One of the key driving forces for employing WBG technologies by industries is the reduced size of power converters. A power converter stores the energy from an input source temporarily in capacitors and/or inductors, and deliver it to the output load continuously and repetitively. The number of such energy-transfer repetitions per second is referred to as switching frequency \( f_{SW} \). WBG devices enable HF operation of power converters, and by increasing the frequency in power conversion, one needs a smaller temporary energy storage to transfer the same amount of power. This is illustrated in Figure 1.4a symbolically, in which the capacitors and inductors are conceptualized as water containers. By increasing the water transfer rate, smaller containers are required to transfer a similar volume of water within a definite time span.

Employing GaN transistors in recently commercialized phone and laptop chargers, which are alternating current (AC)-direct current (DC) power supplies, has significantly reduced the size and weight of those products. Figure 1.4b compares the size and weight of 60-W chargers based on GaN and Si, in which the GaN-based charger offers 35% smaller volume and about 50% less weight [16]. Such a huge size reduction can be achieved without sacrificing the conversion efficiency or power quality.

Figure 1.3 – Comparison of JFOM and BFOM for different semiconductors. The values are normalized by the numbers derived for Si.
Chapter 1. Introduction

Figure 1.4 – Advantage of high switching frequencies for reducing the size and weight of power converters. (a) Conceptualizing inductors and capacitors by water containers. By increasing \( f \), a smaller energy storage is required to transfer the same amount of power. Here, we have drawn an analogy between energy transfer using inductors/capacitors in a power converter, and water transfer using containers. (b) Comparison of 60-W chargers based on Si and GaN technologies. Using GaN has enabled a significant reduction in size and weight of AC-DC supplies.

Electric vehicle (EV) market is constantly growing, and transition towards SiC and GaN technologies could be one of the most promising investments in the sector. Any efficiency boost and size/weight reduction in motor drives, battery chargers (especially in the case of on-board chargers) and DC-DC converters, directly results in longer ranges or less charging times for EVs. Figure 1.5 presents the SiC-based motor drive used in Tesla Model 3. As a pioneer in EV manufacturing, Tesla has been employing SiC technology since 2018 [17].

In Figure 1.6, a comparison is made between motor drives based on two technologies: Si insulated-gate bipolar transistors (IGBTs) and SiC MOSFETs. In this case, using SiC technology has enabled a reduction in switching losses and cooling effort, which not only has boosted the efficiency of the drive, but also

Figure 1.5 – SiC MOSFETs are being employed by EV manufacturers for motor drive applications. Tesla Model 3 designers have been using SiC FETs for EV drive system since 2018 [17, 18]
1.2 Motivation and Challenges

Pushing the limits of efficiency and power density to the maximum using modern power converters based on WBG technologies is the core objective and main motivation of this thesis.

Application of such power converters in several areas such as EVs, rail industry, data center supplies, consumer electronics and renewable energy generation can potentially save tremendous amounts of energy (up to several tens of TWh/year) from being lost in the form of heat [14, 15, 21, 22].

Over and above that, SiC/GaN-based power electronics systems are the key enablers for emerging applications in the future, and help bringing them one step closer to an everyday life reality. Here is a list

Table 1.1 – Comparison of performance and characteristics of inverters based on Si IGBTs and SiC MOSFETs for the 200-kW motor drive application [19]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Si-IGBT Inverter</th>
<th>SiC-MOSFET Inverter</th>
</tr>
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<tbody>
<tr>
<td>Output Power</td>
<td>kW</td>
<td>200</td>
<td>220</td>
</tr>
<tr>
<td>Maximum ( f_{SW} )</td>
<td>kHz</td>
<td>16</td>
<td>24</td>
</tr>
<tr>
<td>Weight</td>
<td>kg</td>
<td>15</td>
<td>9.1</td>
</tr>
<tr>
<td>Volume</td>
<td>l</td>
<td>14.3</td>
<td>10</td>
</tr>
<tr>
<td>Peak Efficiency</td>
<td>%</td>
<td>98%</td>
<td>99.1%</td>
</tr>
<tr>
<td>Efficiency @ Max. Power</td>
<td>%</td>
<td>96.8%</td>
<td>98.2%</td>
</tr>
<tr>
<td>Power Density</td>
<td>kW/l</td>
<td>14</td>
<td>22</td>
</tr>
</tbody>
</table>

Figure 1.6 – Comparison of Si-IGBT and SiC-MOSFET technologies for a 200-kW motor drive application. The inverter based on SiC MOSFETs has several advantages, including higher efficiency, smaller size and lighter weight, which all are of great importance to EV manufacturers.

has significantly reduced its volume (by 30%) and weight (by 40%) without for even a higher output power [19]. Table 1.1 compares the most important parameters of the two designs, in which the power density-the ratio between the power and the converter volume-has increased by about 60% as a result of employing SiC technology.

By using GaN technologies, even 50/60-Hz inverters could be designed to achieve extremely high efficiencies and large power densities. After announcement of IEEE and Google Little Box Challenge in 2014, several inverter designs were demonstrated with unprecedentedly high power densities between 120 to 220 W/inch\(^3\) and efficiencies well above 95% [20].
Chapter 1. Introduction

of examples for such applications which can benefit the most from WBG technologies:

- **High-speed transportation systems:** Figure 1.7a shows a conceptual vertical take-off and landing (VTOL) electric aircraft [23], and a high-speed hyperloop prototype system is shown in Figure 1.7b [24]. The two key parameters for any power electronics system used in such applications are efficiency and power density. Higher efficiencies and power densities directly improve the commuting ranges and reduce the generated heat, which is of great significance to those systems,

![VTOL electric aircraft](a)

![Hyperloop transportation](b)

![LVDC Grid](c)

Figure 1.7 – Power electronics based on WBG technologies offer high efficiencies and large power densities, which enable the emergence of new applications such as (a) VTOL electric aircrafts, (b) hyperloop transportation and (c) DC transformers for future DC grids.
1.2. Motivation and Challenges

especially hyperloop pods within vacuum tunnels.

- **LVDC distribution networks**: Continuous increase in renewable DC power generation such as solar energy and fuel cells on the one hand, and growth in number of DC power consumers including EV batteries, light-emitting diode (LED) lighting systems, data centers, consumer electronics etc. on the other hand, make it advantageous to realize DC grids, which remove the unnecessary AC-DC rectification stages. Such a DC grid is presented in Figure 1.7c. The power point of this architecture is that DC-DC converters, known as DC transformers, can provide a much better controllability and protection for DC grids, compared to that of 50/60-Hz transformers for AC grids [25]. So far, a main drawback for implementation of such DC grids has been the lower efficiencies of DC-DC converters compared to the AC 50/60-Hz transformers. Nonetheless, DC-DC converters based on WBG can overcome the efficiency barriers and enable more-than-ever efficient DC transformers.

To reveal the full potential of WBG technologies in designing high efficiency and high power density converters, a deep knowledge-from understanding the unique characteristics of WBG semiconductors, up to the level of passive element design, electromagnetics considerations, topology enhancement, control at high frequency, and accurate measurements-is a must [20, 21, 26–29]. To put it more precisely, the main challenges can be summarized as:

1. Lack of information about the most important characteristics of WBG transistors in their datasheets and models for HF, very-high-frequency (VHF) and pulsed power applications, including:
   - Effect of gate-drive conditions and DC-link voltage ($V_{DC}$) on the voltage and current switching speeds.
   - The difference between soft-switching and hard-switching operation on the transistor gate loss.
   - Dynamic ON-state resistance degradation and its variation over various blocking voltages (relevant only for GaN transistors).
   - Output-capacitance losses and their variations with the excitation frequency (relevant to soft-switching topologies).

2. Recent literature has demonstrated the superiority of GaN and SiC technologies over their Si counterparts [22, 30–34]; nonetheless, differences between HF and VHF performance of various WBG technologies requires more investigations. As a result, circuit designers have a relatively limited knowledge about the performance differences in various WBG transistor technologies. This becomes more important by taking into account the large differences between performance of devices with various structures and materials.

3. Shortcomings of traditional device characterization methods and systems in measuring high-speed, HF and VHF performance of devices is a major limitation. Establishing novel methods and low-parasitic measurement setups are necessary for overcoming the two aforementioned challenges.

4. Due to bandwidth and accuracy limitations of electrical probes, efficiency and loss measurements for HF circuits can be inaccurate to measure electrically, especially for high-efficiency converters and high-quality sub-components (e.g. magnetics). Therefore, alternative methods have to be developed for precise measurement of component-level and system-level losses and efficiencies.
**Chapter 1. Introduction**

5. Although WBG devices have a clear advantage of reduced losses in hard-switching applications \[20, 33\], for pushing the limits of efficiency and power density, soft-switching topologies are required to eliminate switching losses and enable higher switching frequencies. Applying soft switching and maintaining it at high frequencies for a wide operational range is challenging. That is to say, lack of straightforward soft-switching enhancement methods for HF power converters in terms of topology and control is a major challenge. To be specific, losing soft switching at high frequencies could lead to excessive losses and risk of device failure, and employing topologies and control strategies for extension of soft-switching operation is of great importance. To name a few complications, not only the soft-switching extension should preserve power density, but also it should be feasible to implement at high frequencies, where digital controllers fall short of expectations.

6. Necessity for multi-dimensional parallel optimizations in terms of devices, magnetic design, printed-circuit-board (PCB) layout, cooling and control for achieving simultaneously high efficiencies and large power densities, which are typically two opposing objectives.

### 1.3 Thesis Outline

The thesis in Chapter 2 primarily focuses on accurate methods for voltage rise rate and current rise rate measurements of high-speed GaN and SiC transistors for pulsed-power applications. We highlight the effect of different drive conditions and DC-link voltages on device switching speed. Next in this chapter, major sources of soft-switching losses for HF WBG transistors are identified, and precise methods for quantification and evaluation of those losses are presented for frequencies up to 40 MHz. This chapter further presents a comprehensive comparison between commercial GaN and SiC devices with similar current and voltage ratings for their loss behavior at similar operating conditions.

Chapter 3 provides a summary of the most important performance metrics of HF magnetic materials. Existing loss evaluation methods for HF inductors and transformers are overviewed, and the pros and cons of each method are briefly discussed. This chapter is a prerequisite of Chapters 4 and 5.

In Chapter 4, a novel dual-chamber calorimeter with an unprecedented accuracy and measurement range is proposed for accurate measurement of low losses in power electronics components (e.g. HF magnetics) and efficiency evaluation of highly-efficient power converters. An additional method based on temperature mapping of the elements of a circuit is presented, with a case study example for assessment of gate losses and their distribution over different components in VHF power circuits.

Chapter 5 applies the knowledge from the previous chapters, and introduces control strategies for realizing DC-DC converters with extremely high efficiencies and power densities. First, we propose an enhanced dual-active-bridge (E-DAB) converter, optimized for extended voltage gains at HF, achieving a peak efficiency of 97.4% and a power density of 10 kW/l (or 164 W/inch³). Next, a new operation mode in boost converters based on rectification of repetitive impulses is introduced, enabling a zero-voltage switching (ZVS) operation at different voltage gains. Followed by several optimizations in inductor
The proposed converter concepts and analyses reveal the enormous potential of WBG technologies for pushing the limits of conversion efficiency and power density in power electronics systems. By highlighting various technology limitations and offering accurate measurement methods, not only power electronics designers are able to accurately predict, optimize and evaluate the performance of their designs, but also valuable insights and tools are provided to device engineers to evaluate and improve the key characteristics of GaN and SiC technologies for HF and VHF applications.

Chapter 6 concludes the thesis and provides suggestions for further research in this field.

1.4 Scientific Contributions

The research content presented in this thesis has been published in peer reviewed journals and international conferences:

■ Journal Articles:


■ Conference Proceedings:

Chapter 1. Introduction


Other Contributions:


2 WBG Device Characterization for Pulsed and Soft-Switching Applications

WBG technologies enable faster switching speeds and higher switching frequencies. Faster switching speeds are desirable for pulsed power applications. This chapter initially focuses on the characterization of WBG technologies for their switching speeds under different driving and DC-link conditions, proposing accurate electrical measurement methods to quantify their fast switching transients. Higher switching frequencies translate into reduced size of passive components (i.e. inductors and capacitors) [35]. Resonant and quasi-resonant topologies enable extremely high switching frequencies for power conversion, as they operate the transistors in soft-switching mode [36]. In the second part of the chapter, we propose methods to capture major sources of soft-switching losses in WBG transistors for HF and VHF applications up to 40 MHz. The presented measurements in the chapter enable the comparison of different GaN and SiC transistors for their performance in pulsed power systems as well as the study of their loss behavior in HF power conversion.

In Chapter 5, we use this knowledge to develop high-efficiency soft-switching DC-DC converters based on novel operation modes to maximize their efficiency and power density.

2.1 Switching Speed Characterization for Pulsed Power Applications

2.1.1 Introduction

Voltage rise rate, $VRR = \frac{dv}{dt}$, and current rise rate, $CRR = \frac{di}{dt}$, are the most important characteristics of WBG transistors to study for pulsed-power applications. VRR directly affects the rise time and fall time of an impulse and having transistors with large VRR values is essential to the generation of narrow pulses (e.g. of a few nanoseconds) with high repetition rates. For instance, tuning VRR is fundamental to electroporation (or electroporpermeabilization), a technique in bio-medicine and microbiology which takes advantage of electrical pulses to increase the permeability of a cell membrane for absorption of chemicals, drugs, or DNA [37, 38]. Adjustment of VRR is also of great importance in hard-switching power converters (to limit switching losses) and motor drives (to prevent premature insulation failure of motor windings). Likewise, a particular attention should be paid to CRR capabilities of WBG technologies. Light detection and ranging (lidar) is a technology that is widely used in 3D mapping, distance measurement and navigation systems such as those for autonomous EVs. For lidar drive systems, a higher CRR enables higher resolutions and accuracies as well as faster measurements and less computational efforts [39].
Double-pulse test (DPT) method has been widely used to characterize the switching transients and losses in power switches [40,41]. Electrical schematic of DPT circuit is presented in Figure 2.1, in which the transistor is exposed to two consecutive pulses: the first pulse (turn ON) is to charge the inductor and in the second pulse, the measurement is performed. Capturing fast transients and some specific phenomena (as it will be discussed later in the chapter) could be inaccurate using this method, for the following reasons:

- A typical DPT circuit utilizes a current probe (or a shunt resistor) in its power loop to measure the current waveform. Not only the current measurement bandwidth (BW) can be a severe limitation for fast GaN and SiC transistors, but also due to the intrusive nature of this current measurement, the addition of parasitic inductance and loading effects can result in erroneous measurements [42–44]. Furthermore, the added parasitic capacitances due to the inductor and the diode (as well as diode reverse recovery) in a DPT circuit can degrade the accuracy of the measurements.

- Test results obtained from a DPT test might vary largely based on the applied test conditions such as soaking (blocking) time and duty cycle ($D$). This could be a source of controversy, especially when DPT is applied for evaluating the dynamic degradation of channel resistance [45]. This phenomenon will be explained further in the second part of this chapter.

To overcome these limitations, we propose techniques to quantify the VRR and CRR for fast WBG transistors, and we extract CRR without the need to measure any current waveforms. Furthermore, unlike the DPT method, no additional components such as diodes and inductors are used in the VRR and CRR measurements presented in this section. Thanks to the straightforward nature of the measurements, the methods can be applied to various transistor technologies, which help comparing their performance under similar conditions. Table 2.1 lists four transistors of the same current ratings and breakdown voltages ($V_{BR}$), but different technologies, including GaN, SiC, Si and silicon super-junction (Si-SJ). In the following, we are going to explain the methods used to measure VRR and CRR, and compare the switching speeds of the transistors presented in Table 2.1 according to the methods.

Figure 2.1 – Typical DPT circuit and its limitations for high-frequency and high-speed switching characterization.
Table 2.1 – FETs selected for VRR and CRR measurement and their specifications

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Technology</th>
<th>$V_{BR}$ (V)</th>
<th>$I_D$ (A)</th>
<th>$V_{GS}$ (V)</th>
<th>Capacitance (pF)</th>
<th>$R_G$ (Ω)</th>
<th>$R_{DS(ON)}$ (mΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GS66508T</td>
<td>GaN</td>
<td>650</td>
<td>30</td>
<td>72</td>
<td>6</td>
<td>260</td>
<td>65</td>
</tr>
<tr>
<td>SCT3080AL</td>
<td>SiC</td>
<td>650</td>
<td>30</td>
<td>75</td>
<td>18</td>
<td>571</td>
<td>39</td>
</tr>
<tr>
<td>STW38N65M5</td>
<td>Si</td>
<td>650</td>
<td>30</td>
<td>120</td>
<td>10</td>
<td>3000</td>
<td>74</td>
</tr>
<tr>
<td>NTHL110N65S3F</td>
<td>Si-SJ</td>
<td>650</td>
<td>30</td>
<td>69</td>
<td>10</td>
<td>2560</td>
<td>50</td>
</tr>
</tbody>
</table>

$C_{ISS} = C_{GD} + C_{GS}$

$C_{OSS} = C_{GD} + C_{DS}$
Chapter 2. WBG Device Characterization for Pulsed and Soft-Switching Applications

2.1.2 Voltage Rise Rate Evaluation

A setup including a 1-GHz, 5-GS/s MDO3104 oscilloscope and attenuators, as presented in Figure 2.2, was used to measure VRR for the transistors presented in Table 2.1. Figure 2.3a demonstrates the four-layer PCB for GS66508T GaN transistor evaluation with minimized gate and power loop inductances. The circuit schematic is shown in Figure 2.3b, which consists of two transistors (of the same part number) connected in a half-bridge arrangement. The transistors are driven by isolated gate drivers SI8271, with complementary pulse-width modulation (PWM) signals. Propagation delays of 30 ns (typical) and 60 ns (maximum) are reported for the gate driver, which were considered to properly drive the complementary switches.

Switch node of the half bridge is connected to the 50-Ω termination of the oscilloscope via two attenuators with characteristic impedances of 50 Ω, each providing 20 dB of attenuation (the equivalent of 100 times attenuation in voltage amplitude). The attenuator network, which is presented in Figure 2.3c, consists of a high-power DC to 7 GHz (102-NMFP-20) and a low-power DC to 18 GHz (ATT-0219-20-NNN-02) attenuator. This configuration provides a low-parasitic load and voltage measurement at the same time. Although system BW was limited to 1 GHz (limited by the oscilloscope BW), it was still sufficient for capturing rise times of approximately 400 ps.

For each measurement, the low-side device (FET2 here) was kept at OFF state, and the high-side device (FET1) was turned ON for measuring the VRR.

Figure 2.4 shows the captured voltage waveforms of the switch node (or equivalently \(v_{DS}\), the drain-to-source voltage for the low-side transistor). In all the measurements, a 1-Ω gate resistance (\(R_G\)) was
2.1. Switching Speed Characterization for Pulsed Power Applications

Figure 2.3 – VRR measurement PCB for the GaN transistor, its schematic and the attenuator. (a) PCB design for half bridge with isolated gate drivers and minimum parasitic inductance for the GS66508T GaN device. (b) The half bridge and measurement configuration for VRR measurements. FET<sub>2</sub> is kept at OFF state, and FET<sub>1</sub> is turned ON for measuring the VRR. (c) 50-Ω attenuator arrangement for termination of high-voltage pulses into the 50-Ω internal resistance of the oscilloscope.

placed between the gate driver and the transistor gate. The waveforms have been synchronized (i.e. their gate-to-source voltages, \(v_{GS}\), start rising at the same time). The waveforms correspond to the turn-ON transient of the high-side FET, which results in \(V_{DS}\) of the low-side transistor to rise from 0 to the DC-link voltage (i.e. 400 V in this case). As it can be observed, the GaN transistor achieves the highest VRR and minimum turn-ON delay. The SiC device has a relatively lower VRR, but a larger turn-ON delay. This delay is due to the higher gate capacitance and higher internal gate resistance of the SiC transistor compared to the GaN counterpart. The Si and Si-SJ devices exhibit a different behavior. Due to their large input capacitances (\(C_{iss}\)), they start the transition towards ON state with several nanoseconds of delay. After that, the voltage gradually increases, and only after a few tens of nanoseconds, Si and Si-SJ transistors are able to fully drive the switch-node voltage to 400 V. The poor reverse recovery of the body diode in these transistors is a major drawback, which not only results in longer transition times, but also increases the switching losses in power converters [30]. Due to this fundamental limitation, Si and Si-SJ FETs are not suitable for HF operation. For this reason, we only proceed with SiC and GaN transistors in the Table 2.1 to measure their VRR and CRR.

High VRR values result in shorter overlaps between the transistor current and voltage at the onset of switching, which in turn can reduce switching losses (in the case of hard switching) [46]. However, increasing the VRR can cause several issues such as electromagnetic interference (EMI) in power
Chapter 2. WBG Device Characterization for Pulsed and Soft-Switching Applications

Figure 2.4 – Comparison of voltage rise rate for four different power semiconductor technologies, as presented in Table 2.1. Gate signals are synchronized. The GaN transistor performs the fastest switching transient with the minimum turn-ON delay due to its lowest $C_{ISS}$. The large reverse recoveries and large gate capacitances are two major drawbacks of Si and Si-SJ transistors, hindering their application at high switching frequencies.

Figure 2.5a shows the 3D plot for VRR variation with respect to $V_{GS}$, $V_{DC}$ and $R_G$ for the GS66508T GaN transistor. All the VRR values are extracted based on the 40%-60% (of peak voltage) criterion. The increase in each of the aforementioned parameters results in an increase in the VRR. The VRR can be tuned over a wide span from 16.7 V/ns up to 208 V/ns.

The waveforms in Figure 2.5b illustrate the dependence of VRR on $V_{GS}$, when an external $R_G = 10 \, \Omega$ is used at a 400-V DC-link voltage. The $R_G$ variation also influences VRR substantially, as presented in Figure 2.9c for a 5-V gate supply voltage and 400-V DC-link voltage. By increasing the DC-link voltage, the voltage transitions become faster, as shown in Figure 2.5d for a fixed $R_G = 10 \, \Omega$ and $V_{GS} = 5 \, V$.

A similar set of measurements were performed for the SCT3080AL SiC transistor, with its results shown in the 3D plot of Figure 2.6a, in which the $V_{GS}$ is increased from 15 V to 24 V, DC-link voltages vary between 100 V to 400 V and the $R_G$ value is changed from 1 \Omega to 20 \Omega. By increasing each of the parameters, the VRR is increased continuously from a minimum of 3.1 V/ns to a maximum of 28 V/ns.

Figure 2.6b shows the transient switch-node voltage waveforms for various $V_{GS}$ values at a fixed external $R_G = 10 \, \Omega$ and a DC-link voltage of approximately 400 V. By increasing the gate supply voltage, VRR is increased. A similar trend is observed when $R_G$ is reduced at a fixed gate supply voltage of 5 V, as shown in Figure 2.6c. Also, by increasing the DC-link voltage, and for fixed gating conditions, VRR is increased. Figure 2.6d presents such a trend for $R_G = 1 \, \Omega$ and $V_{GS} = 18 \, V$. 

converters or premature failure of the winding insulation in motor controlled by variable-speed drives or transformers [47–49]. Therefore, it is necessary to investigate major influencing parameters in switching transition speed of WBG devices. In the following, we measure the VRR of GaN and SiC transistors with different external gate resistances and for different gate supply and DC-link voltages and demonstrate how these parameters can be varied to control the voltage transition speed.
2.1. Switching Speed Characterization for Pulsed Power Applications

Figure 2.5 – VRR measurements of the GS66508T GaN transistor. (a) 3D plot of the results for sweeps in $V_{GS}$, $V_{DC}$ and $R_G$. (b) Sweep in $V_{GS}$ at $V_{DC} = 400$ V and $R_G = 10$ Ω. (c) Sweep in $R_G$ at $V_{GS} = 5$ V and $V_{DC} = 400$ V. (d) Sweep in $V_{DC}$ at $V_{GS} = 5$ V and $R_G = 10$ Ω.
Figure 2.6 – VRR measurements of the SCT3080AL SiC transistor. (a) 3D plot of the results for sweeps in $V_{GS}$, $V_{DC}$ and $R_G$. (b) Sweep in $V_{GS}$ at $V_{DC} = 400$ V and $R_G = 1$ Ω. (c) Sweep in $R_G$ at $V_{GS} = 18$ V and $V_{DC} = 400$ V. (d) Sweep in $V_{DC}$ at $V_{GS} = 18$ V and $R_G = 1$ Ω.
2.1.3 Current Rise Rate Evaluation

The setup for capturing the CRR of the GaN and SiC transistors without any actual current measurements is presented in Figure 2.7. For this measurement, the DUT is placed in series between the DC link capacitor bank and a resistive load, as shown in the schematic of Figure 2.8a. The input of the circuit is connected to the DC link via a $RC$ network, in which $R_{CH}$ and $C_{CH}$ are the charging resistor and capacitor, respectively. $R_{CH}$ is a 50-kΩ high-voltage resistor which limits the current from the DC link in case of transistor failure (short circuit) to protect the input DC supply. The load consists of a stack of 60 high-power thick-film resistors in parallel (360-Ω each), as shown in Figure 2.8a. Figure 2.8b shows the actual load resistance ($R_{LOAD}$) and its series parasitic inductance ($L_{PAR}$) measured up to 12 MHz using an E4990A Keysight impedance analyzer. The resistance preserves a constant value of 6 Ω, and the effect of $L_{PAR}$ is negligible as its impedance does not affect the CRR measurement accuracy within the BW required for this test. The FET under test is turned ON using an isolated gate driver (SI8271), and the voltage over the resistive load ($v_{LOAD}$) is measured with a 1-GHz TPP1000 voltage probe connected to the 1-GHz 5-GS/s MDO3104 oscilloscope. Since the transistor is in series with the resistive load, the transistor current can be extracted as $v_{LOAD}/R_{LOAD}$.

Figure 2.9a shows the 3D plot for CRR variation with respect to $V_{GS}$, $V_{DC}$ and $R_{G}$ for the GaN device, ranging from 1.5 A/ns up to 9.25 A/ns. The CRR values were extracted from the slope of the $v_{LOAD}/R_{LOAD}$ curve at 50% of its peak value. The waveforms in Figure 2.9b show the dependence of CRR on $V_{GS}$ when an external $R_{G} = 1$ Ω was used at a 400-V DC-link voltage. The change in CRR for different $R_{G}$ values is presented in Figure 2.9c for an 8-V gate supply voltage and 400-V DC-link voltage. By increasing the DC-link voltage, current transitions typically become faster, as shown in Figure 2.9d for a fixed $R_{G} = 1$ Ω and $V_{GS} = 8$ V.

A similar set of measurements were performed for the SCT3080AL SiC transistor, with the results shown in the 3D plot of Figure 2.10a, in which $V_{GS}$ ranges from 18 V to 24 V, DC-link voltage varies between

![Figure 2.7 – Current rise rate evaluation setup.](image-url)
100 V to 400 V and $R_G$ is changed from 1 Ω to 20 Ω. CRR for the SiC device varies between 0.34 A/ns and 1.28 A/ns, which is almost one order of magnitude lower than that of the GaN device. Figure 2.10b shows the load voltage waveforms for various $V_{GS}$ values at a fixed external $R_G = 1$ Ω and a DC-link voltage of 400 V. By increasing the gate supply voltage, CRR was typically increased. A similar trend was observed by reducing the $R_G$ at a fixed gate supply voltage of 24 V, as shown in Figure 2.10c. It is important to mention that the peak of $v_{LOAD}$ is smaller than the DC-link voltage (i.e. 400 V), which could be attributed to the transistor current saturation. Figure 2.10d presents different load voltage transients when the DC-link voltage was varied between 100 V to 400 V, with $R_G = 1$ Ω and $V_{GS} = 24$ V.
2.1. Switching Speed Characterization for Pulsed Power Applications

Figure 2.9 – CRR measurements of the GS66508T GaN transistor. (a) 3D plot with sweeps in $V_{GS}$, $V_{DC}$ and $R_G$. (b) Sweep in $V_{GS}$ at $V_{DC} = 400$ V and $R_G = 1$ Ω. (c) Sweep in $R_G$ at $V_{GS} = 8$ V and $V_{DC} = 400$ V. (d) Sweep in $V_{DC}$ from 100 V to 400 V at $V_{GS} = 8$ V and $R_G = 1$ Ω.
Figure 2.10 – CRR measurements of the SCT3080AL SiC transistor. (a) 3D plot with sweeps in $V_{GS}$, $V_{DC}$ and $R_G$. (b) Sweep in $V_{GS}$ at $V_{DC} = 400$ V and $R_G = 1$ Ω. (c) Sweep in $R_G$ at $V_{GS} = 24$ V and $V_{DC} = 400$ V. (d) Sweep in $V_{DC}$ from 100 V to 400 V at $V_{GS} = 24$ V and $R_G = 1$ Ω.
2.1. Switching Speed Characterization for Pulsed Power Applications

2.1.4 Conclusion

In this section, we first highlighted the importance of switching speed measurements for different applications in pulsed power and power electronics systems. Next, we introduced single-pulse measurement methods to evaluate VRR and CRR without the need for any current measurements or using extra components in the power loop. The methods can be used as a standard practice for accurate comparison of switching speed in various power semiconductors, as it was illustrated for Si, Si-SJ, SiC and GaN transistors of the same current and voltage ratings.

Si and Si-SJ devices are not suitable for high switching speeds due to the poor reverse recoveries of their body diodes. Furthermore, Due to their large input capacitances, they start the transition towards ON state with several nanoseconds of delay, after which the voltage transition occurs gradually over a few tens of nanoseconds.

The GaN transistor achieved an order-of-magnitude higher CRR compared to the SiC device (a maximum of 9.25 A/ns versus 1.28 A/ns), making it the preferred choice for lidar driving systems.

Similarly, the GaN transistor obtained an order-of-magnitude larger VRR compared to its SiC counterpart (a maximum of 208 V/ns versus 28 V/ns). The fast switching capability of WBG devices is a double-edged sword; it is highly favorable to specific pulsed-power applications, but undesirable in other domains such as motor drives, as high VRR values can expose motor windings to the risk of premature insulation failure.

To that end, the effect of drive conditions and DC-link voltages on VRR and CRR of GaN and SiC transistors was investigated in fine details, where we showed how various parameters such as $R_G$ and $V_{GS}$ can be adjusted to reduce the switching speeds to as low as 3.1 V/ns and 16.7 V/ns for the SiC and GaN transistors, respectively.

In the case of hard-switching converters, VRR and CRR affect switching losses and generated levels of EMI. For instance, a higher VRR shortens the overlap between voltage and current waveforms at the onset of switching, which in turn can reduce the switching loss. Therefore, the presented investigation is of great utility to addressing the trade-offs between switching losses and EMI issues in hard-switched converters, especially those operating at high switching frequencies.
2.2 Soft-Switching Loss Characterization for HF Power Conversion

2.2.1 Introduction

As it was discussed in the previous part of the chapter, the reduced $C_{\text{ISS}}$ in WBG transistors is a key factor contributing to high-speed switching. Together with their smaller ON-state resistance ($R_{\text{DS(ON)}}$), WBG devices enable efficient operation at high frequencies [50, 51]. At such frequencies, soft-switched topologies, especially those designed for ZVS, can potentially achieve very high efficiencies [26, 36, 52–55]. Chapter 5 provides examples of these devices being employed in soft-switching DC–DC converters with high efficiencies [26, 52, 53, 56–58]. GaN and SiC devices are also great choices for wireless power transfer and radio-frequency amplification [59, 60].

For achieving high efficiencies and large power densities, low levels of EMI and proper design of passive components, especially magnetics, become crucial [26, 53, 61, 62]. Criteria for an optimum HF magnetic design will be discussed in great depth in Chapters 3 and 5.

This part of the chapter focuses on the main sources of losses in soft-switched WBG transistors where we demonstrate straightforward measurement methods to precisely measure and compare those losses in various WBG technologies. Figure 2.11 presents the loss breakdown of a soft-switched WBG transistor, including conduction loss ($P_{\text{CON}}$), output capacitance ($C_{\text{OSS}}$) loss ($P_{\text{O}}$), and gate loss ($P_{\text{G}}$), which at HF reduce the system efficiency significantly and expose WBG devices to the risk of thermal runaway [45, 50, 63–65].

The main challenge in determining losses of soft-switched WBG transistors is that manufacturer datasheets either lack sufficient information or present data that are not applicable to a soft-switching case. Furthermore, SPICE models neglect major sources of HF losses, leaving power electronics engineers with no solid evaluation methods to predict or optimize the performance of converters based on WBG devices at HF and VHF ranges.

In the following sections, we use novel methods in combination with existing measurement techniques to quantify soft-switching losses of WBG transistors at HF and VHF. By applying the proposed loss measurement approaches, a detailed and insightful comparison is made between commercial GaN and

![Figure 2.11 – Major sources of losses in a soft-switched WBG transistor are gate loss, output capacitance loss and conduction loss. Various WBG technologies exhibit significantly different loss behaviors at HF and VHF, which are precisely measured and comprehensively analyzed in this part of the chapter.](image-url)
2.2. Soft-Switching Loss Characterization for HF Power Conversion

Table 2.2 – Characteristics of the Evaluated WBG Transistors

<table>
<thead>
<tr>
<th>ID</th>
<th>Part Number (Technology)</th>
<th>$V_{BR}$ (V)</th>
<th>$I_D$ (A)</th>
<th>$Q_G$ (nC)</th>
<th>$R_{DS(ON)}$ (mΩ)</th>
<th>$C_{OSS}$ (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1</td>
<td>GS66508T (p-GaN-gated)</td>
<td>650</td>
<td>30</td>
<td>5.8</td>
<td>50</td>
<td>65</td>
</tr>
<tr>
<td>T2</td>
<td>PGA26E07BA (GaN GIT)</td>
<td>600</td>
<td>31</td>
<td>5</td>
<td>56</td>
<td>71</td>
</tr>
<tr>
<td>T3</td>
<td>TP65H050WS (GaN Cascode)</td>
<td>650</td>
<td>36</td>
<td>16</td>
<td>50</td>
<td>130</td>
</tr>
<tr>
<td>T4</td>
<td>SCT3060AL (SiC)</td>
<td>650</td>
<td>39</td>
<td>58</td>
<td>60</td>
<td>85</td>
</tr>
<tr>
<td>T5</td>
<td>MSC060SMA070S (SiC)</td>
<td>700</td>
<td>37</td>
<td>56</td>
<td>60</td>
<td>138</td>
</tr>
<tr>
<td>T6</td>
<td>UF3C065080K3S (SiC Cascode)</td>
<td>650</td>
<td>31</td>
<td>51</td>
<td>80</td>
<td>62</td>
</tr>
</tbody>
</table>

1 Typical value at 25 °C
2 Reported at 400 V

SiC devices of similar current and voltage ratings (see Table 2.2), with their various losses being evaluated up to 40 MHz.

2.2.2 Gate Loss

At high and very-high frequencies, gate loss cannot be neglected and its accurate evaluation becomes crucial for cooling and gate driver design. One can employ a resonant gate driver to recover a part of energy stored in a transistor $C_{ISS}$ by using inductors and clamping circuits [57, 66–68]. Such solutions result in larger driver size, limitations in timing and $D$ as well as extra inductor losses. Furthermore, as Figure 2.12 shows, $C_{ISS}$ values in SiC and GaN devices are highly nonlinear with $V_{GS}$ (unlike in Si-based devices); this can make resonator tuning based on datasheet parameters a challenge at a given frequency. Due to their simpler designs, push-pull gate drivers are still preferable for many HF applications based on WBG transistors, in spite of the fact that the applied hard gating results in the entire stored energy in the gate capacitance to be dissipated in gate drive path.

The problem, however, is that the reported gate charge ($Q_G$) values in datasheets are measured as transistors are subjected to a hard turn ON, as illustrated in Figure 2.13; thus, those measurements are not applicable to a soft-switching operation. It is because the gate-to-drain capacitance, $C_{GD}$, has different initial electric charges when the transistor is turned ON in either case [27, 65, 69, 70]. Furthermore, the reported $Q_G$ refers to a typical value, and the actual value can vary largely between transistors of a same part number. Figure 2.14a presents the measured input capacitance for a sample of twenty GaN transistors with the same part number of GS66508T, when drain was shorted to source and a small-signal voltage at 1-MHz was applied over the gate and source terminals. By extracting the equivalent $Q_G$ for 5-V and 6-V gate-drive voltages, Figure 2.14b reveals a variation of higher than ±20% in gate charge over the 99th percentile (±3σ) of the samples. Thus, a straightforward method for evaluation of gate loss in individual devices is extremely useful, whether for the purpose of design optimization and loss breakdown, or for cherry-picking devices based on their gate loss.

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Figure 2.12 – Comparison of $C_{ISS}$ versus $V_{GS}$ for Si, SiC and GaN semiconductor technologies. Values are normalized. Large variation of $C_{ISS}$ with $V_{GS}$ in WBG transistors poses a challenge to resonant gate driver design at high frequencies.

To address the aforementioned issues, we demonstrate an accurate and simple method based on a small-signal $C_{ISS}$ versus $V_{GS}$ measurement to evaluate gate loss in a wide variety of WBG transistors. We further verify the method for its accuracy by applying electrical power measurements and thermal evaluations.

By modeling the gate as $C_{ISS}$ in series with a gate resistance and a gate driver resistance, $P_G$ for push–pull gate drivers can be formulated as the total energy required to charge $C_{ISS}$ from $V_{OFF}$ to $V_{ON}$, multiplied by $f_{SW}$ as

$$P_G = Q_G (V_{ON} - V_{OFF}) f_{SW}$$  \hspace{1cm} (2.1)
2.2. Soft-Switching Loss Characterization for HF Power Conversion

Figure 2.14 – Statistical analysis of input capacitance variation between WBG devices with a same part numbers. (a) Variation in $C_{ISS}$ versus $V_{GS}$ in a sample of twenty GS66508T GaN transistors. A variation of more than 20% necessitates a precise measurement method for accurate estimation of gate losses, especially at high frequencies, when the gate losses in WBG devices become considerably large. (b) Statistical parameters of soft-switching $Q_G$ for 5-V and a 6-V driving conditions. The measurements were performed using a Keysight E4990A impedance analyzer and a 16047E 120-MHz test fixture, when the drain of each transistor was shorted to its source, to emulate a ZVS condition.

where $Q_G$ for soft-switched transistors can be extracted as

$$Q_G = \int_{V_{OFF}}^{V_{ON}} C_{ISS}(v) \, dv \quad (2.2)$$

$C_{ISS}$ in (2.2) is the small-signal capacitance measured over voltage using an impedance analyzer when the drain is shorted to the source to emulate ZVS condition. In Figure 2.15, $C_{ISS}$ is measured at 1 MHz using
Figure 2.15 – Small-signal $C_{ISS}$ versus $V_{GS}$ for $T_1$–$T_6$ measured at 1 MHz. The gate in most of the transistors can be regarded as a $RC$ circuit. Device $T_2$ exhibits a capacitive behavior for low voltages, and as $V_{GS}$ increases, it performs similarly to a diode with an ON-state current, as indicated by the gradient shading under its $C_{ISS}$-versus-$V_{GS}$ curve. An E4990A impedance analyzer and a 16047E test fixture, where the shaded areas under $C_{ISS}$-versus-$V_{GS}$ curves represent the soft-switching $Q_G$. $T_2$ is a gate-injection transistor (GIT) whose gate presents capacitive behavior at low drive voltages and behaves as a diode in ON state at higher voltages. Other transistors behave only as a nonlinear capacitor over the measured voltage range.

Figure 2.16 – Time-domain gate-to-source voltages for $T_1$–$T_6$, driven with their nominal gate drive conditions at 5 MHz.
To verify the small-signal prediction of gate losses based on (2.1), we operated the transistors from 100 kHz up to 5 MHz (at \(D = 50\%\)) with their drains shorted to their source terminals. Figure 2.16 presents the time-domain gate-to-source voltages at 5 MHz. The real \(P_G\) values were extracted by electrical and thermal methods. In the electrical method, we used the cross product of the current and voltage of the gate-driver supply, measured with Fluke 87V multimeters. Figure 2.17 presents the time-domain \(V_{GS}\) waveforms for \(T_1\) to \(T_6\) at 5 MHz, measured using a TPP1000 1-GHz voltage probe. To drive \(T_2\), a constant current-source driver (AN34092B) recommended by the \(T_2\) manufacturer was used. To drive the other transistors, we employed a wide-voltage-range gate driver (SI8271). Although the gate drive resistances were similar, settling times for \(v_{GS}\) waveforms in the GaN devices \(T_1\) and \(T_2\) were much smaller than those of SiC devices, indicating the superiority of GaN transistors for HF and VHF applications over their SiC counterparts.

Additionally, an accurate thermal method based on temperature mapping was developed to verify gate losses up to 30 MHz, whose details are discussed in Chapter 4, under Section 4.2.

Both methods verified the accuracy of the presented small-signal measurement approach. Figure 2.18a presents the error of using \(Q_G\) from (2.2) for \(P_G\) evaluation with respect to the real measured gate losses at 5 MHz. A consistent error of less than 10% was observed for transistors \(T_1\), \(T_4\), \(T_5\), and \(T_6\), whose gates can be modeled as \(RC\) circuits. \(T_2\) and \(T_3\) exhibited a frequency-dependent \(C_{ISS}\), as shown in Figure 2.18b. Also, the excessive increase of \(C_{ISS}\) with \(V_{GS}\) in \(T_2\) at higher driving voltages [see Figure 2.15] and the resonance observed at about 6.5 MHz for \(T_3\) suggest that their gates cannot be modeled simply as \(RC\) circuits. Hence, the evaluation method is not applicable and one needs to perform a direct loss measurement, as performed in Figure 2.17.

The demonstrated method based on \(C_{ISS}\)-versus-\(V_{GS}\) measurement provides invaluable information for gate loss estimations with low errors in soft-switched transistors and selecting low-loss devices for HF and VHF applications. For instance, \(T_1\) exhibited the smallest \(P_G\) and is best suited for VHF operation.
2.2 Characterization for Pulsed and Soft-Switching Applications

-40 -30 -20 -10 0 10 20 30 40

Error (% of Real \(P_G\))

\(f = 5\) MHz

Higher than real \(P_G\)

Lower than real \(P_G\)

\(T_1\) \(T_2\) \(T_3\) \(T_4\) \(T_5\) \(T_6\)

0 1000 2000 3000

\(C_{ISS}\) (nF)

\(f_{OSC}\) (MHz)

\(T_1\) (GaN) \(T_3\) (GaN) \(T_4\) (SiC) \(T_6\) (SiC)

(a)

(b)

Figure 2.18 – (a) The error of using the small-signal \(Q_G\) from \(2.2\) for \(P_G\) evaluation at 5 MHz. The recommended method shows a consistent error of less than 10%. Symbol “⋆” indicates that the recommended method is not applicable to \(T_2\) and \(T_3\) since their gates cannot be modeled as RC circuits. (b) The frequency dependence of \(C_{ISS}\). \(T_2\) and \(T_3\) devices exhibit a strong variation in \(C_{ISS}\), signifying that their gate cannot be modeled as RC circuits. \(T_3\) shows a resonance at about 6.5 MHz.

It is important to mention that the parasitic inductance in series with the transistor can result in a resonance which is not inherently existing in the device. To avoid such spurious measurements, any parasitics should be minimized and the test frequency (or oscillation frequency \(f_{OSC}\) of the impedance analyzer) has to be much smaller than the resonance frequency [71].

As a summary, we discussed that the standard gate-charge information in WBG device datasheets are extracted using hard-switching tests. As this standard information can result in large errors in the estimation of \(P_G\) for soft-switching transistors, it is extremely important to include the \(C_{ISS}\)-versus-\(V_{GS}\) measurements in manufacturer datasheets, especially for those of WBG devices.

2.2.3 Output Capacitance Loss

Charging and discharging of transistor output capacitance in the case of resonant topologies with soft switching can possibly lead to a nonrecoverable energy loss in WBG transistors operating at HF and VHF [50, 63, 72, 73].

Different approaches are proposed in the relevant literature to measure those losses. In [63], a thermal approach is used to study soft-switching output capacitance losses. However, the existence of additional loss mechanisms and voltage oscillations could significantly limit the method’s applicability for high \(dv/dt\) values. Sawyer–Tower (ST) circuit is another tool used to extract the losses by using a power amplifier and applying a large-signal (sinusoidal) excitation over the device output capacitance [74, 75]. Despite the simplicity of ST method, the limited BW of power amplifiers and risk of device thermal runaway hinder its application at high frequencies and high \(dv/dt\) conditions [63, 64]. The analysis of the nonlinear resonance (NR) between the transistor \(C_{OSS}\) and a series HF inductor has been proposed by Samizadeh et al. to extract the losses and overcome the aforementioned shortcomings [64]. The NR
method can extract $P_O$ for large voltages and $dv/dt$ values as high as 100 V/ns, which are achievable with WBG power transistors [76].

The related power dissipation can be formulated as

$$P_O = f E_{DISS} \quad (2.3)$$

where $f$ is the operation frequency and $E_{DISS}$ is the energy dissipated in each charging/discharging cycle of $C_{OSS}$.

$E_{DISS}$ based on ST method can be extracted from the $v_{DS}$-versus-$q$ curve as described in Figure 2.19. The reference capacitor ($C_{REF}$) has a constant capacitance which is used to extract the transistor output charge (based on the principle that series capacitors store equal electric charges). A Keysight 33600A function generator, a Falco Systems WMA-300 amplifier, and a HF step-up transformer were employed to generate a 400-V peak-to-peak voltage over the device under test (DUT) with its gate shorted to the source, as shown in Figure 2.20a. The selection criteria for the reference capacitor and other circuit parameters are broadly discussed in [75] by Perera and his colleagues.

Figure 2.20b shows $v_{DS}$-versus-$q$ curves corresponding to charging and discharging of $C_{OSS}$ measured using ST method at 100 kHz. The larger the deviation between the charging and discharging curves, the higher is the value of $E_{DISS}$. Observed hysteresis patterns vary between GaN and SiC devices. The cascode GaN transistor $T_3$ exhibited the highest $E_{DISS}$, which was about 2 µJ (the equivalent of 200 mW of power dissipation when being soft switched at 100 kHz). $E_{DISS}$ in $T_1$ was almost negligible, and the hysteresis in $T_2$, which occurred at high voltages, amounted to $\approx 0.4$ µJ. $E_{DISS}$ in SiC devices $T_4$ and $T_6$ was $\approx 0.3$ µJ, whereas charging and discharging of $T_5$ did not result in any power dissipations.

As described earlier, NR method takes advantage of the $LC$ resonance between device output capacitance and a series inductor (the resonance occurs after the transistor is turned OFF and the inductor current is interrupted). This method is suitable for higher frequencies, and the resonance frequency (or test frequency) can be adjusted based on the magnitude of the employed series inductance with $C_{OSS}$. For this set of measurements, the transistors were placed in series with high quality ($Q$) factor inductors (air-core inductors with $Q > 100$ at each test frequency) to evaluate $E_{DISS}$ for $f > 1$ MHz. In Chapter 3 we discuss more about $Q$ factor and how it can be measured for HF inductors. The PCB design used for $E_{DISS}$ measurements of $T_1$ based on NR method is presented in Figure 2.21a.

![Figure 2.19 – ST circuit and methodology for measurement of output capacitance loss.](image-url)

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Figure 2.20 – Evaluation of transistor output capacitance loss using ST Method. (a) Test setup for the ST experiment composed of a DUT, a HF step-up transformer, a WMA-300 power amplifier and a Keysight 33600 A function generator. The 1-GHz voltage probes are used to extract $v_{\text{REF}}$ (directly) and $v_{\text{DS}}$ (indirectly by subtracting $v_{\text{REF}}$ from the applied AC source voltage). (b) $V_{\text{DS}}$-versus-$q$ results based on ST measurements for $T_1$–$T_6$ at 100 kHz and 400 V.

Figure 2.21b illustrates the extracted time-domain $v_{\text{DS}}$ waveforms based on NR method at two very different test frequencies. The dashed curve in each plot is the mirrored half curve of $v_{\text{DS}}$ versus time (the rising portion). The deviation between the mirrored curve and the actual $v_{\text{DS}}$ in its falling half is an
indicator of how large the $E_{\text{DISS}}$ is. The corresponding $E_{\text{DISS}}$ for each case can be extracted as [64]

$$E_{\text{DISS}} = \frac{1}{2L} \left( \left( \int_{t_0}^{t_1} v_{\text{DS}}(t) \, dt \right)^2 - \left( \int_{t_1}^{t_2} v_{\text{DS}}(t) \, dt \right)^2 \right)$$

(2.4)

In this expression, $L$ is the inductance in series with the DUT which participates in a resonance with the transistor $C_{\text{OSS}}$, and intervals $(t_0, t_1)$ and $(t_1, t_2)$ correspond to the charging and discharging of the $C_{\text{OSS}}$, respectively (see Figure 2.21a).

By merging the results obtained from the two methods, we quantified $E_{\text{DISS}}$ over a wide frequency range from 100 kHz up to 40 MHz, as illustrated in Figure 2.22. ST results correspond to the measurements for $f < 1$ MHz and NR method was employed for all the measurements above 1 MHz [64, 74, 75, 77].

GaN device T$_1$ exhibited an exponential increase of $E_{\text{DISS}}$ over $f$, with negligible energy losses at low frequencies. $E_{\text{DISS}}$ values from [73] are also presented in Figure 2.22 for T$_1$ for its two different packages (top cooled, bottom cooled) at 5 and 10 MHz, which are in the same range as presented here. The exponential increase of $E_{\text{DISS}}$ in T$_2$ starts after about 5 MHz. The cascode device T$_3$ has large $E_{\text{DISS}}$ values even at low frequencies, and its $E_{\text{DISS}}$ increases at higher frequencies. As shown before, SiC devices have large $v_{\text{GS}}$ settling times and in practice, their $E_{\text{DISS}}$ values become important only for lower frequencies (i.e. below 5 MHz).

Datasheets provide $C_{\text{OSS}}$ stored energy ($E_{\text{OSS}}$) which can be useful for the evaluation of hard-switching losses; however, $E_{\text{DISS}}$ information for soft-switching transistors is missing. Hence, the presented results and methods are suggested to be used by device manufacturers to improve their datasheets, as such results are of great significance to soft-switching VHF designs based on WBG technologies, and in specific, GaN-based applications in which the devices can potentially switch at tens of MHz.

### 2.2.4 Conduction Loss

Dynamic $R_{\text{DS(ON)}}$ degradation in a power transistor leads to higher resistance values immediately after a turn-ON transition. GaN devices are susceptible to degradation of dynamic $R_{\text{DS(ON)}}$ as a result of charge-trapping effect of electrons [45, 78–80]. This phenomenon leads to extra power dissipations, which are here referred to as dynamic losses ($P_{\text{DYN}}$). OFF-state voltage (or blocking voltage) seems to have the highest impact on the dynamic $R_{\text{DS(ON)}}$ behavior of soft-switched GaN transistors [51].

As discussed in [45], to avoid large under/over-estimations of dynamic $R_{\text{DS(ON)}}$ degradation compared to the actual device performance in a power converter, it is crucial to accurately specify blocking times and perform the experiments over repetitive switching cycles. Also, due to the uncertainties involved in DPT measurements (see Section 2.1), we employed an alternative technique called pulsed-IV. By using the pulsed-IV system (AMCAD in this case), each DUT was subjected to $V_{\text{GS}}$ (using gate probe iTest AM213) and $V_{\text{DS}}$ (using 1 kV/30 A drain probe PIV AM241) excitations as shown in Figure 2.23a, with 5-µs ON-time and 15-µs OFF-time intervals at a 50-kHz pulse repetition rate.

Time-domain $R_{\text{DS(ON)}}$ measurements for the GaN device T$_1$ are presented in Figure 2.23b for $V_{\text{DS}} = 0$.
Figure 2.21 – Evaluation of transistor output capacitance loss using NR Method. (a) NR test board including a gate drive and a high-Q-factor inductor in series with the DUT. The test circuit schematic and the important timings are specified. (b) Time-domain $V_{DS}$ for $T_1$–$T_6$ using NR method at two distant frequencies. The dashed curves are the mirrored rising half of the generated pulse. The higher the deviation of a dashed curve from a solid-lined curve is, the more $E_{Diss}$ a transistor has.
2.2. Soft-Switching Loss Characterization for HF Power Conversion

V, 100 V, and 400 V. To capture the actual $R_{DS(ON)}$ and minimize the effect of noise, we averaged the resistance values over a 1-µs interval, after the settling time of the measurement tool was reached (i.e., 2.5 µs after the device was turned ON, as indicated by the measurement windows within Figures 2.23a and 2.23b). $R_{DS(ON)}$ was measured at 20% of the rated current (i.e., at about 6 A).

Figure 2.24 shows the normalized $R_{DS(ON)}$ variation versus $V_{DS}$ (the reference for normalization is the measured $R_{DS(ON)}$ value at $V_{DS} = 0$ V). In T1, we observed a degradation of 25% at 400 V, and even larger at lower voltages, whereas T2 and T3 exhibited lower degradations. From Figure 2.24, we can conclude that dynamic $R_{DS(ON)}$ degradation is almost absent in SiC transistors T4 to T6.

2.2.5 Discussion

Figure 2.25 summarizes the soft-switching losses of devices T1 to T6 from 100 kHz up to 5 MHz, based on the loss breakdown described in Figure 2.11. The devices were driven at their respective nominal gate voltages with $D = 50\%$ and at 20% of their rated currents for $V_{DS} = 400$ V. The losses due to conduction were divided into $P_{CON}$ and $P_{DYN}$. $P_{DYN}$ represents only the contribution of the dynamic $R_{DS(ON)}$ degradation, whereas $P_{CON}$ considers the measured value of $R_{DS(ON)}$ at $V_{DS} = 0$. Although $P_{DYN}$ in GaN devices increases with frequency, the variation is small and negligible within the presented frequency range of Figure 2.25 [79, 80].

Figure 2.25 illustrates that GaN device T1 has the lowest overall losses. Despite exhibiting the most severe $R_{DS(ON)}$ degradation at 400 V [also see Figure 2.24], due to its low gate and output capacitance losses, T1 offers the best performance for VHF applications, especially those with low duty cycles or small currents.

---

Figure 2.22 – $E_{DISS}$ versus frequency for T1–T6 measured using ST ($f < 1$ MHz) and NR ($f > 1$ MHz) methods. ’■’ marks in the plot for T1 refer to the measured values from reference [73] for GS66508T and GS66508B GaN transistors.
Relatively higher gate loss and the requirement for special gate-drive circuitry impose limitations on HF application of GaN transistors such as T\textsubscript{2}, whose gate behaves similarly to a diode at large \( V_{GS} \) values.

A cascode arrangement enables higher threshold voltage \((V_{TH})\) in \( T_3 \) (compared to GaN devices \( T_1 \) and \( T_2 \)) and lower gate loss in \( T_6 \) (compared to SiC devices \( T_4 \) and \( T_5 \)); however, higher output capacitance losses were observed for these cascode devices, even at low frequencies. Besides, the existence of gate resonance in \( T_3 \) [see Figure 2.18b] as well as its negative resistance behavior [81] can make this device prone to large-signal instabilities [82].

![Diagram of Pulsed-IV Method](image)

**Figure 2.23 – Dynamic \( R_{DS(ON)} \) measurement using pulsed-IV method with a 50-kHz pulse repetition rate.**

(a) The DUT was subjected to \( V_{GS} \) and \( V_{DS} \) pulses and the resistance was measured in the measurement window after the settling time of the setup was reached. (b) \( R_{DS(ON)} \) variation for \( T_1 \) at OFF-state \( V_{DS} \) of 0 V (no voltage stress), 100 V, and 400 V.
2.2. Soft-Switching Loss Characterization for HF Power Conversion

Figure 2.24 – Normalized $R_{DS(ON)}$ versus $V_{DS}$ for transistors $T_1$ to $T_6$. $R_{DS(ON)}$ versus $V_{DS}$ pattern varies between GaN devices. SiC transistors exhibit a negligible increase of $R_{DS(ON)}$. Devices are subjected to 20% of their nominal current. $R_{DS(ON)}$ was captured 2.5 µs after the DUT was turned ON, and was averaged over a 1-µs interval to reject the effect of noise.

Figure 2.25 – Soft-switching loss components versus frequency for transistors $T_1$–$T_6$ at their nominal $V_{GS}$ when the transistors were subjected to $V_{DS} = 400$ V and 20% of their nominal current. The comparison is of great significance for selection of WBG devices, converter efficiency optimization and proper design of cooling systems.
2.2.6 Conclusion

As it was shown in the first part of this chapter, WBG FETs based on GaN and SiC achieve fast switching speeds which in turn enables HF operation of these devices. At high frequencies, the elimination of switching losses, especially at turn-ON transients, becomes crucial [54, 83]. As it will be shown in Chapter 5, topologies such as phase-shifted full-bridge (PSFB) [61], dual-active-bridge (DAB) [52, 53], and soft-switched boost converters [26, 55] take advantage of ZVS for efficient HF operation with removing the hard-switching losses. Since datasheets lack information on soft-switching losses in WBG transistors, it is important to investigate such losses in further details. The presented loss measurements in the second part of this chapter emulated a ZVS operating condition.

By combining the estimation methods and measurements presented in the previous subsections, one can extend the loss evaluation to higher frequencies (even up to 40 MHz). We demonstrated a comprehensive loss breakdown analysis for soft-switching operation of WBG transistors. A small-signal input capacitance measurement versus gate-to-source voltage was used to evaluate gate losses under soft-switching conditions, and its accuracy was experimentally verified. By using a combination of ST (for \( f < 1 \text{ MHz} \)) and NR methods (for \( 1 \text{ MHz} < f < 40 \text{ MHz} \)), we demonstrated the variation of large-signal \( C_{\text{OSS}} \) losses for different technologies over a wide frequency range. To obtain an overall view of the losses, we further compared the degradation of dynamic \( R_{\text{DS(ON)}} \) and its dependence on the OFF-state voltage using the standard pulsed-IV method. Three SiC and three GaN devices of the same current (\( \approx 30 \text{ A} \)) and voltage (\( \approx 650 \text{ V} \)) were evaluated and compared for their gate loss, output capacitance loss, and conduction losses up to 5 MHz.

The most severe \( R_{\text{DS(ON)}} \) degradation and the lowest gate loss were observed in a p-GaN-gated device (T₁), which is the best choice for VHF applications, especially those with low duty cycles or small currents. The cascode arrangement in SiC and GaN devices offers advantages such as increased threshold voltage and reduced gate loss. However, their output capacitance losses are aggravated at high frequencies, which limit their high-frequency low-loss performance. The demonstrated measurement methods are general and can be used to evaluate the soft-switching losses in other WBG transistors. Given the diversities of WBG technologies, this chapter intended to present the major trade-offs in selecting a power device to maximize the system efficiency, and to carry out a proper thermal design for high-frequency soft-switching applications. This analysis is also insightful for device engineers to design high-performance power transistors for HF and VHF applications.
Magnetic Design for High-Frequency Power Applications

3.1 Introduction

The main purpose of using magnetic cores is to increase the inductance density which can potentially reduce the size and weight of power electronic circuits. This chapter primarily discusses the criteria for choosing magnetic components for HF power conversion by introducing the sources of magnetic losses. Next, the most common approaches for loss evaluation and optimization of HF magnetics - from simulation tools to small-signal quality factor measurements - are presented. The chapter is a prerequisite for Chapters 4 and 5, in which we introduce accurate measurement methods for low losses in HF converters and magnetic components, and optimize inductors and transformers for high efficiencies and high power densities in HF power converters, respectively.

3.2 Sources of Magnetic Losses

For power converters which operate based on magnetic power transfer, selection of efficient magnetic materials is of great importance to the conversion efficiency and power density. A High-quality magnetic material should have certain properties, including [84]:

- a high relative permeability ($\mu_r$)
- a high saturation magnetic flux density ($B_S$)
- a high electrical resistivity ($\rho_c$)
- a low magnetic coercivity ($H_C$)
- a high Curie temperature ($T_C$)
- low hysteresis and eddy-current losses per unit of volume ($P_V$)
- a high upper operating frequency ($f_H$) or a wide BW.
Chapter 3. Magnetic Design for High-Frequency Power Applications

According to the aforementioned parameters, FOM of a magnetic material can be defined as [84]

$$
\text{KFOM} = \frac{\mu_r \rho_c B_S f_{\text{H} \text{I}}}{P_V}
$$

(3.1)

A higher $\mu_r$ increases inductance for the same core volume and number of winding turns in an inductor. However, to avoid a reduction in $\mu_r$ for soft magnetic materials, their magnetic flux density ($B$) has to be lower than $B_S$. In other words, as $B$ increases, $\mu_r$ drops, and after passing the saturation limit $B_S$, the magnetic material behaves similar to air ($\mu_r \rightarrow 1$).

Eddy currents are formed within conductors which are exposed to a variable magnetic field, based on Faraday’s law. A material with large $\rho_c$ is desirable as it has low eddy-current losses. Magnetic coercivity, $H_C$, determines the ability of a magnetic material to withstand an external magnetic field without becoming demagnetized. Materials with high coercivity are called hard magnets and are used to make permanent magnets for several applications such as brushless and synchronous electrical machines [84]. Soft magnetic materials are typically used as a temporary energy storage in power converters. For these magnetic materials, $H_C$ is a measure of hysteresis losses. The cumulative effect of hysteresis and eddy-current losses can be indicated by $P_V$.

Depending on the material, parameters such as $\mu_r$ and $\rho_c$ could be strong functions of frequency. Therefore, it is desirable to utilize magnetic materials with higher BW, capable of operating efficiently at higher frequencies (or equivalently those materials having higher $f_{\text{H} \text{I}}$).

$T_C$ is the temperature above which certain materials lose their magnetic properties. A magnetic core in power converters must always be operated below its $T_C$.

In the following, we introduce and compare different magnetic materials for their performance at high frequencies.

### 3.3 Magnetic Materials Suitable for HF Applications

Ferromagnetic metals include iron (Fe), nickel (Ni) and cobalt (Co). Materials such as silicon steel (SiFe) and nickel iron (NiFe) exhibit high $B_S$ values (typically > 1 T). Their $\mu_r$ is also large (well above 1000). Nonetheless, they are highly conductive materials (with low $\rho_c$) which hinders their application in the HF domain due to their huge eddy-current losses.

Ferrites are ferrimagnetic materials, which contain elements such as chromium (Cr) and manganese (Mn) which are the neighbors of iron in the periodic table of elements. Their advantage compared to the typical ferromagnetic materials is their higher resistivity ($\rho_c$) at high frequencies, which results in lower eddy currents and consequently lower HF eddy-current losses. To put this advantage in perspective, nanocrystalline cores are limited to frequencies of up to several tens of kHz due to their extremely low $\rho_c$ at HF, whereas ferrites are suitable for frequencies of up to several tens of MHz.

Two of the most promising ferrites for power conversion belong to manganese zinc (MnZn) and nickel
zinc (NiZn) families. Table 3.1 compares the most important material properties for power conversion using these ferrites. MnZn ferrites offer higher inductance values for the same cross-sectional area and number of turns, as their $\mu_r$ is an order of magnitude larger than that of the NiZn; nonetheless, the higher $B_S$ in MnZn ferrites together with their lower $H_C$ are great advantages for efficient and high power density converter design at HF. However, these advantages in MnZn ferrites come at the price of lower resistivity, which results in much higher eddy-current losses compared to the NiZn ferrites. NiZn ferrites typically have four orders of magnitude higher $\rho_c$, which makes them highly suitable for applications with frequencies in the range of tens of megahertz.

### 3.4 Loss Evaluation in Inductors and Transformers

The KFOM presented in (3.1) is insightful for comparing the performance of different magnetic materials without getting into the complex details of each material. Nonetheless, parameters such as $\rho_c$ and $\mu_r$ are variable with frequency, and inductors or transformers based on the very same material can behave very differently over frequency. Besides, actual losses in an inductor or transformer not only depends on the employed material, but also on its geometry and choice of its windings (solid conductor, copper foils, Litz wire etc.). Therefore, it is of great significance to go beyond metrics such as KFOM, and investigate methods for quantifying the losses in magnetic components at different frequencies. In the next two sections, we take a look at the most important and useful tools for performance evaluation of transformers and inductors based on HF magnetic materials.

#### 3.4.1 Simulation Tools

Finite-element analysis (FEA) is a strong tool to analyze magnetic flux density magnitude and its distribution in magnetic cores of different shapes and materials, as well as the current density ($J$) inside various winding structures.

To show the utility of FEA simulations, here we present a HF transformer design for obtaining low losses, suitable for operation in a PSFB DC-DC converter [61]. The converter topology is shown in Figure 3.1a, where a DC input voltage is converted to a HF square-wave signal by the primary-side inverter. This exposes the transformer to a bipolar current excitation. The transformer provides the required voltage step-up/down (12x step-up in this case), and its leakage inductance is responsible for power transfer. The secondary-side transformer voltage is then rectified using a full-bridge diode rectifier and the output current is filtered at the output using an inductor. The primary-side inverter consisted of GaN FETs with
Figure 3.1 – PSFB converter topology utilizing a HF transformer. (a) PSFB topology including a primary-side inverter, a HF transformer and a secondary-side rectifier. (b) The primary-side inverter PCB consists of GaN FETs with high switching frequency capabilities. (c) Secondary-side rectifier consists of SiC Schottky diodes with a zero reverse recovery suitable for HF operation.

fast switching capabilities (as shown in Figure 3.1b, and enabled an excitation frequency of 300 kHz for the HF transformer. The secondary-side rectifier was consisted of SiC Schottky diodes with a zero reverse recovery, to minimize HF diode losses (see Figure 3.1c).

To optimize the system performance, not only a deep knowledge in semiconductor device properties is
3.4. Loss Evaluation in Inductors and Transformers

(a) High-frequency planar transformer (left) consisting of five stacks of 6-layer PCBs (right)

(b) Magnetic flux density norm at 300 kHz

(c) Current density norm at 300 kHz

Figure 3.2 – FEA simulation is a strong tool for design and optimization of magnetic components. (a) A HF planar transformer is realized with stacks of interleaved PCB windings. (b) Magnetic flux density norm; this parameter is an indicator of the magnitude and distribution of core losses. (c) Current density norm; this parameter is highly instrumental for optimizing the winding AC resistance.

...a must (c.f. Chapter 2), but also magnetic components has to be designed with low losses and compact sizes to reveal the full advantage of using WBG devices. Figure 3.2a demonstrates the planar transformer design-whose windings are copper traces of multi-layer PCB stacks—for operation at 300 kHz in the PSFB converter [61]. COMSOL FEA tool was utilized to analyse the amplitude and local distribution of the two most important parameters for HF magnetics, $B$ and $J$, as:

- **Analysis of $B$ for core losses**: To verify the magnitude and distribution of $B$ inside the core, the transformer under full-load operation was simulated, as shown in Figure 3.2b, where the average $B$ was verified to be 14 mT, far below the $B_S$ for the saturation limit of the employed material ($B_S$ for N95 material is greater than 300 mT). The result is an efficient operation of the core. To characterize the converter performance for its transformer losses over different loading conditions, one can also extract $B$ at different loads, as it will be shown with an example in Chapter 5.

- **Analysis of $J$ for winding losses**: Skin and proximity effects increase winding effective resistances,
which limits the efficiency of magnetic components at high frequencies (more on this in the next section). Figure 3.2c shows the short-circuit current density norm for the designed planar transformer. By analysing different winding geometries and interleaving schemes, one can significantly reduce winding resistances at high frequencies [61, 85].

While FEA methods are extremely useful for inductor and transformer optimization [61, 86, 87], they have serious limitations for loss evaluations and fall short of accurate system-level performance evaluation of inductors and transformers. FEA tools (including the example we provided here for the PSFB converter) in general provide single-tone AC excitations. Furthermore, frequency-dependent characteristics of the magnetic materials are complicated to model, especially for non-sinusoidal excitations. Also, modeling winding structures (especially in the case of Litz wires with large strand counts) is not always computationally feasible. Thus, the extracted losses using FEA tools for HF and VHF ranges are prone to various uncertainties. Another major shortcoming of loss estimation based on simulation models is the absence of temperature-dependent effects, which can result in non-realistic and erroneous loss evaluations for magnetic components [88, 89].

### 3.4.2 Quality Factor Measurements

HF inductors are typically exposed to a wide range of frequencies (in the case of converters with frequency modulation, as will be shown in Chapter 5) or high orders of harmonics (in the case of hard switching converters with fast switching transitions). Therefore, their loss behavior over frequency is of great importance. The $Q$ factor of an inductor is an important criterion which quantifies its loss behavior over different frequencies.

To give a better understanding of $Q$ factor, an electrical equivalent circuit of the HF inductor should be considered, as shown in Figure 3.3. To focus mainly on the losses, this model neglects any parasitic capacitances (stray winding capacitances or capacitive effects caused by dielectric behavior of magnetic cores). In the presented circuit, $R_C$ is a non-linear frequency-dependent resistance that represents core losses, which can be divided into [90]:

- Hysteresis loss which is non-linear (with voltage or magnetic flux) and independent from frequency. Larger $H_C$ results in larger hysteresis losses.

![Figure 3.3 – The equivalent circuit of an inductor at high frequencies neglecting the effect of parasitic capacitances. $R_C$ and $R_{AC}$ represent the core and winding losses, respectively.](image)
3.4. Loss Evaluation in Inductors and Transformers

- Eddy-current loss which is frequency-dependent as a result of variation in \( \rho_c \) over frequency.

- Relaxation loss which varies with frequency and occurs due to other physical mechanisms.

\( R_{AC} \) in Figure 3.3 corresponds to winding losses. This term is a frequency-dependent resistance which can be broken down into its two sub-components as:

\[
R_{AC} = R_{COND} + R_{PROX}
\]  

(3.2)

In (3.2), \( R_{COND} \) is called conductive resistance and \( R_{PROX} \) is proximity-effect resistance. \( R_{COND} \) is associated with the DC resistance and the skin effect over the windings, and \( R_{PROX} \) is the result of current crowding caused by external magnetic fields from adjacent conductors [91]. In the case of using Litz wires, \( R_{PROX} \) also includes the additional resistance caused by the external magnetic field from adjacent strands.

By taking into account all the resistances discussed above, \( Q \) factor can be equated as

\[
Q = (2\pi f) \frac{L}{R_C + R_{AC}}
\]  

(3.3)

With an impedance analyzer, one can measure the complex electrical impedance of passive elements such as inductors and capacitors (for instance, we used E4990A impedance analyser for measuring the transistor input capacitance in Chapter 2). The complex impedance then can be used to extract \( Q \) factor for inductors with different core materials, geometries and winding types.

To demonstrate and example, Figure 3.4a presents a PQ32/30 coil former which is used to design single-layer solenoid air-core inductors with different Litz wires, but of similar overall cross-sectional area (i.e. \( \approx 0.53 \text{ mm}^2 \)), as listed in Table 3.2.

The small-signal \( L \) values measured with the E4990A impedance analyser and its 16047E 120-MHz test fixture are in the same range, as shown in Figure 3.4b. Figure 3.4c presents the extracted \( Q \) factor values. Although winding geometry (single-layer solenoid), overall cross-sectional area, and inductance values are similar, \( Q \) factor profile varies largely between inductors with different Litz wires. Thus, Such a small-signal \( Q \) measurement is highly instrumental to the design and optimization of windings in air-core inductors, as it will be shown in Chapter 5. There, we also use \( Q \) factor to compare the leakage inductance loss behavior of HF transformers with different geometries for efficient operation in isolated DC-DC converters.

In the case of a single-tone excitation, \( Q \) factor can be defined as the ratio between the stored energy to
the energy dissipated per cycle of inductor charging/discharging as

\[ Q = 2\pi \frac{\text{energy stored}}{\text{dissipated energy per cycle}} \] (3.4)

Table 3.2 – List of Litz wires used to realize air-core inductors of Figures 3.4a-3.4c

<table>
<thead>
<tr>
<th>Wire type</th>
<th>Strand cross-sectional area (mm²)</th>
<th>Overall cross-sectional area (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S105/AWG40</td>
<td>0.005</td>
<td>0.525</td>
</tr>
<tr>
<td>S165/AWG42</td>
<td>0.0032</td>
<td>0.528</td>
</tr>
<tr>
<td>S675/AWG48</td>
<td>0.000784</td>
<td>0.529</td>
</tr>
<tr>
<td>Single/AWG20</td>
<td>0.5175</td>
<td>0.5176</td>
</tr>
</tbody>
</table>
(3.4) can be used to determine the amount of power loss in air-core inductors. Nonetheless, extraction of losses with the $Q$ measurements using impedance analyzers has several limitations:

- Impedance analyzers are not capable of providing large amounts of active and reactive power to the DUT; therefore, the measured $Q$ factor using impedance analyzers does not take into account the non-linear hysteresis energy losses (which vary with $B$) [92].

- Although $Q$ is extracted over frequency, the excitation signal for measurement is always single tone; consequently, it might not always be useful to evaluate losses, especially for real operating conditions of magnetic components, for instance when they are exposed to square-wave voltages and triangular currents [92].

- The DUT almost never experiences a temperature rise; thus, temperature-dependent losses are not captured [88].

Accurate measurement of losses in magnetic components is a necessary step towards optimizing them for the maximum efficiency and power density, which is the main target of this thesis. Although FEA simulation tools and small-signal $Q$ measurements provide insights about the losses in magnetic components, they have severe shortcomings. In the next chapter, we introduce a calorimeter which is capable of accurately measuring the losses in such components in their real operation conditions in a power circuit.

### 3.5 Conclusion

Accurate measurement of losses at real operating conditions of magnetic components is highly instrumental to the optimization of power converters and design of wide-bandwidth inductors/transformers. FEA and other real-time simulation tools are extremely useful for verification of certain design aspects under simplified modeling assumptions. Nonetheless, magnetic losses are non-linear with $B$ and have dependencies on frequency and temperature; thus simplified models cannot give a general and accurate estimation of losses in these components. Small-signal $Q$ factor was later introduced as a straightforward measurement method to quantify the losses in air-core inductors (in Chapter 5, examples of HF inductor and transformer optimization will be presented using this method). However, it was mentioned that the small-signal $Q$ factor falls short of accurate loss measurements and the results might differ significantly from the HF and VHF large-signal operating conditions. In Chapter 4, we introduce a novel calorimetric measurement method for precise evaluation of losses in magnetic components. Unlike the presented small-signal $Q$ factor measurement method, the calorimeter is capable of capturing the losses while the magnetic component is operating in a real converter. Furthermore, as it will be discussed further, the calorimeter outperforms electrical measurement systems at HF and VHF power conversion systems, when their accuracy and BW become limiting factors for capturing low losses.
In Chapters 2 and 3, we discussed the importance of using high-performance WBG technologies and high-quality passive components (e.g., high-frequency transformers and inductors) to enable ultrahigh efficiencies in high-frequency power conversion [26, 27, 52, 53, 55, 93–96].

However, measuring high efficiencies using electrical methods is often prone to large errors due to insufficient measurement accuracies [97, 98]. Furthermore, electrical measurements, especially current probing, suffer from limited bandwidths, neglecting the effect of high-order harmonics [44, 95]. Loading effects (probe burden), propagation delays between the employed voltage and current probes, and EMI are other limiting factors for precise measurement of losses in various converter building blocks, such as switches with fast transition speeds (as shown in Chapter 2) and HF magnetic components (as discussed in Chapter 3) [97–99].

Calorimetric methods have been used to directly determine losses in the form of generated heat in power converters [98, 100], pulsed-power generators [101], motors and drives [102, 103], and semiconductor devices and passive components [97, 104]. Such approaches can overcome the aforementioned limitations of electrical tools, especially for measurement of low losses in HF and VHF circuits and components.

In this chapter, we propose two methods for accurate loss measurements in various power electronics systems and components. The first part of the chapter focuses on the presentation of a novel dual-chamber calibration-free calorimeter which is capable of measuring losses down to 500 mW in power converters and their sub-components (e.g. inductors and transformers). In the next part, we present a method in which losses of components in a circuit can be extracted based on their temperature mapping, which not only can be used to extract the total loss value, but also provides accurate information about the loss distribution in different parts of the circuit.
Chapter 4. Advanced Calorimetric Techniques

4.1 Calibration-Free Calorimeter for Sensitive Loss Measurements

4.1.1 Introduction

In a calorimetric system, heat-transfer rate ($P$) from the source of power dissipation to the coolant can be determined by

$$ P = \rho \frac{dV}{dt} c_p \Delta T \quad (4.1) $$

in which $\rho$ is the volumetric density of the coolant, $V$ is its volume, $c_p$ is the isobaric specific heat capacity, and $\Delta T$ is the corresponding temperature rise.

Single-chamber open-type calorimeters use air flow meters with temperature sensors at the inlet and outlet of a chamber with air blown on the DUT. This method is simple to implement for measuring large losses [105]. The air parameters, such as $\rho$ and $c_p$, are susceptible to large variations and for reliable measurements, time-consuming calibrations or balance tests must be performed. A balance test is performed with heaters to emulate the operation conditions of the main DUT to compensate for variations in the air properties. Furthermore, the heat leakage through the chamber has to be minimized for a high precision [102].

A double-chamber open-type calorimeter can mitigate the need for calibrations and balance tests [106]. This method is practical for measuring large losses but equalizing the heat leakage between the two chambers remains a challenge, and there is no guarantee that the air flow remains the same in both chambers, depending on the DUT geometry [99].

By using a heat exchanger and transferring the heat to a liquid (e.g. water), one can directly extract the power loss with a single chamber closed-type calorimeter based on (4.1) [98, 105, 107]. Although using water with its large heat capacity increases the settling time in closed-type systems, the accuracy is significantly higher. A single-chamber calorimeter must minimize the heat leakage through the walls, so a double-jacketing technique is used in [98, 100, 105]. Christen et al. [98] reported a good precision of ± 0.4 W for a 10-W loss measurement. This calorimeter is suitable for measuring losses up to 100 W; nonetheless, evaluating smaller losses requires a much higher sensitivity.

In this section, we propose a double-chamber closed-type calorimeter, as shown in Figure 4.1, which overcomes the limitations of the aforementioned methods by the following steps [29, 89]:

1. Reducing the flow rate drastically for achieving a higher sensitivity. The same coolant flows in both chambers; hence, there is no need to measure extremely low flow rates, which is highly challenging [105]. As a result, the sensitivity is high enough to measure losses as low as 500 mW with significantly lower costs.

2. Replacing the time-consuming calibrations, balance tests, and data processing by a real-time calibration for faster loss evaluations.

3. Avoiding the need for a perfect thermal insulation since low levels of heat leakage, if equal for both chambers (which holds in the case of identical chambers here with symmetrical designs), do not
4.1. Calibration-Free Calorimeter for Sensitive Loss Measurements

Figure 4.1 – The proposed dual-chamber calibration-free calorimeter concept. Water flows in identical chambers containing DUT and calibrator, CAL. Heat transfers through heat exchangers (convection) and cold plates (conduction) and water temperature rise is measured across both chambers. The blue lines indicate cold water and red lines represent hot water, after absorbing the energy dissipated in DUT and CAL. The arrow shows the direction of flow. External heat exchangers are used to cool the water down to the ambient temperature.

...introduce measurement inaccuracies.

4.1.2 Methodology

The proposed calorimeter enables geometry-independent loss measurements by transferring the heat to the water through heat exchangers (convection) and cold plates (conduction). Two identical thermally-insulated chambers are placed inside an outer chamber that isolates the calorimeter from the ambient (see Figure 4.1). The water at the ambient temperature flows through the DUT chamber and after absorbing the heat generated by the DUT, gets cooled down to the ambient temperature using an external heat exchanger. The same liquid then flows through the calibration (CAL) chamber and heats up with its dissipated power \( P_{\text{CAL}} \). After exiting the calibration chamber, another external heat exchanger cools down the liquid to the ambient temperature. The entire heat-transfer cycle is repeated until the temperatures reach a steady state. Such a closed loop for the coolant ensures a constant flow in both chambers and eliminates the need for precise flow measurements. Temperature gradients \( T_4 - T_3 \) and \( T_2 - T_1 \) are measured and compared constantly, and a proportional-integral (PI) regulator adjusts \( P_{\text{CAL}} \) such that both chambers have equal steady-state temperature gradients. Thus, the DUT loss, \( P_{\text{DUT}} \), can be derived at steady state as

\[
T_4 - T_3 = T_2 - T_1 \iff P_{\text{DUT}} = P_{\text{CAL}} \tag{4.2}
\]

To avoid a DUT thermal runaway before the steady state is reached and (4.2) can be used for loss evaluation, the cooling capability and sensitivity of the system can be adjusted by changing the water flow rate and fan power of the inner heat exchangers \( P_{\text{FAN}} \).
Table 4.1 – Comparison of the proposed calorimeter with other works in the literature for calorimetric measurement of power losses

<table>
<thead>
<tr>
<th>Reference</th>
<th>System</th>
<th>Type/Coolant</th>
<th>Minimum Power</th>
<th>Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>[105]</td>
<td>Single-chamber</td>
<td>Closed/Water</td>
<td>74.5 W</td>
<td>± 0.5 W</td>
</tr>
<tr>
<td>[106]</td>
<td>Double-chamber</td>
<td>Open/Air</td>
<td>200 W</td>
<td>± 15 W</td>
</tr>
<tr>
<td>[98]</td>
<td>Single-chamber</td>
<td>Closed/Water</td>
<td>10 W</td>
<td>Max{± 0.4 W, 1%}</td>
</tr>
<tr>
<td>This Work</td>
<td>Double-chamber</td>
<td>Closed/Water</td>
<td>500 mW</td>
<td>At 500 mW:+50%/-30%</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>At 15 W: ± 3%</td>
</tr>
</tbody>
</table>

The proposed method requires no prior calibrations or extra data analyses, resulting in faster evaluation times. Table 4.1 compares this method with previous techniques in the literature, where our proposed system extends the measurement range to power levels as low as 500 mW.

4.1.3 System Design

Figure 4.2a shows the outer chamber with dimensions $120 \times 66 \times 70 \text{ cm}^3$, made of polystyrene insulator. The water circuit [see inset of Figure 4.2a] includes a water reservoir connected to a µ-diaphragm pump with a pulsation damper, to stabilize the low flow of the liquid. Low flow rates enable a higher water temperature rise and thus higher sensitivities.

The inner chambers consist of polystyrene boxes with dimensions $48 \times 42 \times 36 \text{ cm}^3$ and are covered with shielding foils to suppress any possible effects of radiated EMI from the DUT on the measurements. To the same end, all the sensors are kept outside the two chambers [see Figure 4.2b]. Inside each of the chambers is an aluminum container to hold the inner heat exchangers and cold plates [see Figures 4.2c and 4.3a]. The DUT is mounted on the cold plate and its hot-spot temperature ($T_{HS}$) is monitored through the aperture in the container using thermal imagers to avoid a thermal runaway. To verify the real-time calibration and its dependence on the DUT geometry, two very different fixtures, $A$ and $B$, were employed, as shown in Figure 4.3b. Fixture $A$ is an array of thick-film resistors mounted on a printed circuit board. The fixture $B$ is a power resistor connected to the cold plate using only one nylon stand-off (with a poor thermal conductivity to the cold plate).

The general system view in Figure 4.4a presents the calorimeter and its mechanical components including the inner and outer heat exchangers and the water pump, with major input (feedback) and output (control) signals. As Figure 4.4b shows, a peripheral management board was designed at the interface between the calorimeter and myRIO-1900 control unit. Analog and digital grounds were separated in this hardware interface, in order to reduce any possible EMI issues. The data acquisition system, which was developed in LabVIEW environment, constantly provided measurements for the real-time regulator as well as the human interface. Moreover, by transferring the data to a computer, all system parameters were recorded for further offline analyses.

Table 4.2 lists a detailed description of the mechanical components, measurement tools, and data acquisition/controller unit used in the system design.
Figure 4.2 – Dual-chamber calorimeter design. (a) The outer chamber and heat exchangers, together with the water circuit. (b) The inner chambers with the aluminum fixtures inside. Shielding foils all over the inner and outer walls of chambers are used to suppress any possible effects of radiated EMI on the measurements. (c) The container holding inner heat exchangers and cold plates. The back-side view of the container shows the calibration resistors mounted on the cold plate.
Figure 4.3 – Test fixtures designed and employed for calibration of the calorimeter. (a) An array of thick-film resistors (Fixture A) and (b) a power resistor mounted on the cold plate using only a nylon stand-off (Fixture B) are used to examine the dependence of the calorimeter measurements on the DUT geometry. To that end, DC calibrations are performed and presented in Subsection 4.1.4.

<table>
<thead>
<tr>
<th>Component</th>
<th>Type</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Water Temp. Sensor</td>
<td>Pt. 100 Class AA</td>
<td>Accuracy ±0.1°C</td>
</tr>
<tr>
<td>μ-Diaphragm Pump</td>
<td>NFB5KTDCB-4</td>
<td>Maximum Pressure: 1 Bar</td>
</tr>
<tr>
<td>Pulsation Damper</td>
<td>FDP06KTZ</td>
<td>Maximum Pressure: 2 Bar</td>
</tr>
<tr>
<td>Cold Plate</td>
<td>416101U00000G</td>
<td>Aluminum Base/ Copper Tubes</td>
</tr>
<tr>
<td>Heat Exchanger (In)</td>
<td>Alphacool XT45</td>
<td>2 Fans</td>
</tr>
<tr>
<td>Heat Exchanger (Out)</td>
<td>Airplex PRO 240</td>
<td>3 Fans</td>
</tr>
<tr>
<td>DC Measurements (Calibration)</td>
<td>Fluke 45</td>
<td>Voltage Accuracy: 0.025% + 6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Current Accuracy: 0.2% + 7</td>
</tr>
<tr>
<td>DC Measurements (Fan Power)</td>
<td>Fluke 87V</td>
<td>Voltage Accuracy: 0.05% + 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Current Accuracy: 0.2% + 2</td>
</tr>
<tr>
<td>Data Acquisition</td>
<td>myRIO-1900</td>
<td>LabVIEW environment</td>
</tr>
</tbody>
</table>
4.1. Calibration-Free Calorimeter for Sensitive Loss Measurements

Figure 4.4 – Control and feedback signals to/from the actuators/sensors. (a) Major input and output signals for the real-time control process and (b) hardware for the controller, including a peripheral management board (left) and myRIO-1900 (right). Data acquisition records the measurements on computer for further offline analyses.
4.1.4 DC Calibrations

DC calibrations were performed to verify that both chambers are identical and to ensure that the measurement method has no dependency on geometry of the tested DUT. In DC calibrations, equal levels of power were dissipated in both chambers and the water temperature gradients over the chambers were measured and compared. The flow rate was adjusted by tuning the power of the μ-diaphragm pump.

As illustrated in Figure 4.5a, using a low flow (the equivalent of minimum pump pressure) enabled a good sensitivity to losses as low as 100 mW with an error of less than 10% up to 10 W. This slight mismatch is attributed to the error in water temperature measurements [see Figure 4.5b]. A minimum $P_{\text{FAN}}$ of 0.3 W was used for a homogeneous air circulation. We repeated DC calibrations for a high flow rate, corresponding to the maximum pump pressure, and an error of less than 10% was maintained for losses down to 1 W, where the water temperature gradient ($\Delta T_{\text{Water}}$) reached the detection threshold of the

![Graph](image)

Figure 4.5 – Steady-state DC calibration results for the calorimeter-Phase 1. (a) Investigating the effect of different water flow rates. Having a low flow increases sensitivity. High flows enable better cooling of the DUT. (b) The higher water flow rate results in lower hot-spot temperature. The overall error is always below 10%.
4.1. Calibration-Free Calorimeter for Sensitive Loss Measurements

Figure 4.6 – Steady-state DC calibration results for the calorimeter-Phase 2. (a) The effect of $P_{\text{FAN}}$ at 5 W and 10 W. (b) Increasing fan power leads to higher steady-state $T_{\text{HS}}$. This parameter is instrumental to measure converters and components with heatsinks for cooling. The error is much smaller than 10%.

sensors. As Figure 4.5b shows, the high flow rate results in lower $T_{\text{HS}}$ for the DUT, which can be tuned to avoid its thermal runaway, depending on the DUT loss level and the overall thermal resistance. $P_{\text{FAN}}$ is a secondary tunable parameter, whereby increasing the air flow, a better convective heat transfer via the inner heat exchangers is achieved.

Figure 4.6a presents the cases where 5 W and 10 W are consumed by the fans. As the chambers are thermally insulated, higher fan powers result in larger steady-state $T_{\text{HS}}$. However, increasing $P_{\text{FAN}}$ results in higher air velocity and, thus, a better convective heat transfer, which is more advantageous for converters and components using heatsinks for their cooling. As Figure 4.6b shows, for $P_{\text{FAN}}$ values of up to 10 W, an error much less than 10% was obtained.

To investigate the dependence of the calorimeter on geometry of the heat source, fixtures $A$ and $B$ were compared in DC calibrations. Even with such an extreme change in the geometry of the heat source and
Figure 4.7 – Steady-state DC calibration results for the calorimeter-Phase 3. (a) The effect of DUT geometry. Due to the low thermal conductivity of the fixture \(B\) to the cold plate, it has a much higher \(T_{HS}\). However, \(\Delta T_{\text{Water}}\) remains similar in both cases, exhibiting no dependence on the DUT geometry. (b) The mismatch errors of less than 10% for losses as low as 100 mW indicate similar designs of the two chambers and repeatability of the measurements.

its coupling to the system, \(\Delta T_{\text{Water}}\) remained similar [see Figure 4.7a] and a maximum error of 10% was obtained [see Figure 4.7b], indicating the independent performance of the calorimeter with respect to the DUT geometry. The higher overall \(T_{HS}\) observed using the fixture \(B\) [as shown in Figure 4.7b] suggests that the heat transfer is dominated by the cold plate. Hence, DUTs with larger losses must have a better thermal coupling to the cold plate by using a thermal interface material. Heatsinks could also be utilized to improve the convective heat transfer.

The mismatch errors of less than 10% for all the DC calibrations show the repeatability of the measurements as well as the identical thermal resistances from the two chambers to the water circuit. Although the water temperature sensors are highly linear within the measured ranges, their limited accuracy is the main source of the observed mismatches.
Figure 4.8 presents time-domain temperature gradients of the DUT and CAL chambers during DC calibration tests \( (P_{\text{FAN}} = 900 \text{ mW}) \). In this case, the power loss varied between 1 W to 8 W, and slow, medium and fast flows were applied. The calorimeter offers high accuracy as well as flexibility for measuring DUTs with different cooling requirements and reduces the measurement times by eliminating any balance tests or data post processing.

### 4.1.5 Power Tracking and Accuracy

Figure 4.9a presents the transient \( \Delta T_{\text{Water}} \) for both chambers, together with the power tracking in CAL, when DUT is dissipating 7.8 W. A PI regulator provided the reference power \( (P_{\text{CAL}}^*) \) to an adjustable DC source to satisfy (4.2), as shown in Figures 4.9b, 4.9c. The system constantly monitored \( T_{\text{HS}} \) in the chambers using infrared (IR) thermometers to limit the power to the CAL and DUT in the possible case of a thermal runaway. The proportional \( (k_P) \) and integral \( (k_I) \) coefficients were tuned using the transfer function of the calorimeter in frequency domain (s-domain) to properly adjust the power tracking transient.

The power is measured by multiplying the voltage and current of the calibrator using a Fluke 45 dual
display multimeter as

\[ P_{\text{CAL}} = (V_{\text{CAL}} \pm \epsilon_V)(I_{\text{CAL}} \pm \epsilon_I) \]  \hspace{1cm} (4.3)

where \( \epsilon_V = 0.025\% \) and \( \epsilon_I = 0.2\% \) are the DC voltage and DC current measurement errors, respectively. At steady state, the temperature rise in the water is linearly proportional to the dissipated power (see the left-side curves in Figures 4.5a, 4.6a and 4.7a, noting that the power is plotted in the logarithmic scale). Based on (4.2) and (4.3), one can extract the tracked power \( P_{\text{TRACK}} \) as

\[ P_{\text{TRACK}} = P_{\text{LOSS}} \left(1 \pm \epsilon_V \pm \epsilon_I\right) \frac{\Delta T_{\text{DUT}} \pm 2\epsilon_T}{\Delta T_{\text{CAL}} \mp 2\epsilon_T} \]  \hspace{1cm} (4.4)

where \( P_{\text{LOSS}} \) is the actual power dissipation and \( \epsilon_T = 0.1 \degree\text{C} \) is the error involved in the water temperature.
4.1. Calibration-Free Calorimeter for Sensitive Loss Measurements

In the first parenthesis of (4.4), the values of $\epsilon_I$ and $\epsilon_V$ are much smaller than unit, and thus are negligible. Figure 4.10 presents the overall measurement error, $\epsilon$, for the proposed calorimeter for the various power dissipations when a low flow rate is applied and $P_{FAN} = 0.3$ W.

The error band shrinks at higher $P_{LOSS}$ values and is expanded at lower powers due to the inaccuracy of the water temperature sensors, as indicated by (4.4). The calorimeter is capable of tracking power losses as low as 500 mW with $+50\%/-30\%$ accuracies. The error is less than 30% for measurements above 1 W and becomes significantly lower at higher power levels.

The system accuracy can be simply improved by using a liquid with lower $c_p$ to generate a higher water temperature rise for the same power dissipation. More precise and pre-calibrated water-temperature sensors effectively improve the accuracy based on (4.4). Better thermal insulation of the inner chambers (to avoid heat leakage) is as important in measuring lower loss levels. Furthermore, using the same concept when the entire DUT is immersed in a dielectric liquid significantly enhances the setup accuracy as well as its cooling capability.

4.1.6 Calorimeter for System-Level Efficiency Measurements

The demonstrated calorimeter significantly improves the accuracy in system-level efficiency measurements for ultrahigh-efficiency power converters in kilowatts power ranges. The actual converter efficiency can
be expressed as

\[ \eta_{\text{ACTUAL}} = \frac{P_{\text{OUT}}}{P_{\text{IN}}} = 1 - \frac{P_{\text{LOSS}}}{P_{\text{IN}}} \]  

(4.5)

where \( P_{\text{IN}} \) and \( P_{\text{OUT}} \) are the actual average input and output powers, respectively, and \( P_{\text{LOSS}} \) is the actual power dissipation. For a DC–DC converter, one needs to use a high-precision digital multimeter (DMM) to measure \( P_{\text{IN}} \) and \( P_{\text{OUT}} \) by the multiplication of currents and voltages, and extract the efficiency using (4.5) as

\[ \eta_{\text{DMM}} = \frac{P_{\text{OUT}}(1 \mp e_V \mp e_I)}{P_{\text{IN}}(1 \pm e_V \pm e_I)} \]  

(4.6)

The main advantage of using calorimeters for efficiency measurements is that they can directly measure \( P_{\text{LOSS}} \), which is unfeasible to do with electrical methods. Based on (4.5), the calorimeter measures the

Figure 4.11 – Comparison of the error in efficiency measurements using a high-precision DMM (Fluke 87V) and the calorimeter system for a power converter operating at 1 kW. Shaded areas indicate the uncertainty ranges in each method. The calorimeter avoids spurious efficiency measurements for ultra-efficient power converters in the range of kilowatts.
4.1. Calibration-Free Calorimeter for Sensitive Loss Measurements

The efficiency of the same power converter as

\[ \eta_{\text{CAL}} = 1 - \frac{P_{\text{LOSS}} (1 \pm \epsilon)}{P_{\text{IN}} (1 \pm \epsilon_V \pm \epsilon_I)} \]  

(4.7)

in which \( \epsilon \) represents the calorimeter overall error in the loss measurements, extracted from (4.4) (see Figure 4.10).

Figure 4.11 compares the evaluated efficiencies for a power converter operating at 1 kW, when using the proposed calorimeter and a high-precision DMM with \( \epsilon_V = 0.05\% \) and \( \epsilon_I = 0.2\% \). The calorimeter avoids spurious efficiency measurements (which might sometimes exceed 100\%), and provides a much better accuracy for low amounts of losses.

4.1.7 Calorimeter for Component-Level Loss Measurements

In Chapter 3, we argued that it is crucial to quantify the large-signal losses in components with high-frequency AC excitations such as inductors and transformers. For such cases, the losses can be very inaccurate to be measured electrically. Also, simulation tools and small-signal \( Q \) evaluations are accurate.

In this section, we use the proposed calorimeter to measure large-signal losses in HF inductors. A two-winding method is generally used to measure core loss, in which a transformer is made by adding a secondary sensing winding to the inductor [108]. This method is susceptible to large errors due to large phase discrepancies [109]. Although the method has been improved by introducing capacitive and inductive cancellation methods [110], still several sources of error exist, including the parasitic inductance of current measurement probe (or shunt resistor) and interwinding and intrawinding transformer capacitances. Especially for measurement of low-permeability cores in high-\( Q \) inductors, the aforementioned errors become significant. For instance, to provide a proper coupling between the two windings of the equivalent testing transformer in low-permeability magnetic cores, a bifilar winding structure is necessary, which can significantly increase the interwinding capacitance.

The proposed calorimeter overcomes those shortcomings at tens of MHz and unlike most electrical methods which extract inductor losses only under sinusoidal excitations, it can measure these losses under real power circuit operations, regardless of the applied waveform shapes, frequencies and transition speeds. The only trade-off is the increased measurement times compared to the electrical methods. It is worth mentioning that the proposed calorimetric concept can save time by removing extra balance tests and further compensations which are typical and time consuming in other calorimetric methods.

Here, we compare two toroidal inductors with a similar inductance, \( L \), for their small-signal \( Q \) factors and large-signal core and winding losses. Figure 4.12a demonstrates the setup for small-signal measurements of \( L \) and \( Q \) using an E4990A Keysight impedance analyzer with 16047E 120 MHz fixture.

As Figures 4.12b, 4.12c present, an air-core inductor is compared with a low-permeability NiZn ferrite (material 68). Based on Figures 4.12d, 4.12e, both of the inductors maintain a 6.9 \( \mu \)H inductance up to several MHz; however, the ferrite 68 material has a much higher \( Q \). As it was comprehensively explained
Figure 4.12 – Small-signal inductor $Q$ factor measurements. (a) E4990A impedance analyzer with 16047E test fixture were used to measure the small-signal properties of two inductors with (b) an air-core and (c) a ferrite 68 core. (d) The inductors have equal inductances up to several MHz. (e) presents their small-signal $Q$ factors. The amplitude of the AC signal was set to 500 mV, and the DC bias was zero. Although the small-signal $Q$ factor is a good indicator of HF performance in air-core inductors, it is not accurate for loss estimation in inductors with cores.

In Chapter 3, small-signal $Q$ is a good measure of winding losses for air-core inductors; nonetheless, a large-signal excitation is required to evaluate the total loss, including that of the NiZn core.

To that end, a GaN-based inverter was used as a large-signal excitation source. Figure 4.13a shows the
4.1. Calibration-Free Calorimeter for Sensitive Loss Measurements

Figure 4.13 – Large-signal inductor excitation setup for loss measurement experiment. (a) a controller using TMS320F28379D digital signal processor (DSP) generates PWM signals to drive a GaN-based inverter. To make a resonance, the inductor was placed in series with a high-Q (mica) capacitor. (b) shows the setup for calorimetric measurement, and (c) shows the electrical measurement setup using MSO64 oscilloscope, voltage (TPP1000) and current (TCPA300 Amplifier + TCP305) probes.

Two sets of measurements were performed to extract the large-signal losses. In Figure 4.13b configuration, the calorimeter was used to measure losses, when the GaN inverter and the resonant capacitor were kept outside of the calorimeter, and only the inductor was placed in the DUT chamber.

A second configuration, as shown in Figure 4.13c, was used to measure the losses electrically. By using a voltage probe with 1 GHz of BW and a current probe with BW = 50 MHz, the overall core and winding...
losses were extracted for each charging/discharging cycle. To compare the results from both configurations and verify the calorimeter accuracy, the test excitation frequency was intentionally relatively low (i.e. 277 kHz), so that the BW of the employed electrical probes would not be a limiting factor.

The calorimetric measurement results are presented in Figures 4.14a and 4.15a, in which the inductors were subjected to current excitations at a fundamental frequency of 277 kHz with different amplitudes.

Figure 4.14a presents IR thermographs of the ferrite 68 inductor with peak currents ranging from 3 A to 3.59 A, as shown in Figure 4.14b. The thermographs were captured after the thermal steady state was reached for each case. The measured losses with the calorimeter are plotted in Figure 4.14c, in which the uncertainty ranges are indicated by red bars.

Figure 4.15a shows the IR thermographs of the air-core design, with peak currents ranging from 3 A to 4 A (see Figure 4.15b). The air-core inductor losses, shown in Figure 4.15c, have a slight dependence on the current amplitude; whereas, the ferrite 68 inductor losses increase significantly with current excitation amplitude (cf. Figures 4.14c and 4.15c).

In parallel to each calorimetric measurement and at the same temperature conditions, an electrical
Figure 4.15 – Calorimetric measurements for losses of the air-core inductor at 277 kHz. (a) Inductor thermographs at different peak currents ranging from 3 A to 4 A. (b) Current waveforms and (c) the losses measured by the proposed calorimeter. The error bars are indicated for each measurement. A low water flow rate and an inner fan power of 300 mW were applied.

A low water flow rate and an inner fan power of 300 mW were applied. Figures 4.16a-4.16d show the $B$-$I$ curves extracted for the ferrite 68 inductor, and Figures 4.17a-4.17d present those for the case of the air-core inductor.

The $B$-$I$ curves were used to calculate the overall losses as

$$P_E = \int I \, dB$$

(4.8)

$P_E$ incorporates hysteresis loss (as the major source of power dissipation in ferrite cores) and winding loss. It should be emphasized that for any electrical measurements to be valid, the thermal steady-state for the inductor has to be reached before the measurement is performed electrically. Otherwise, temperature-dependent loss parameters are not taken into account, resulting in large errors.

Figures 4.18a, 4.18b compare the extracted losses using the dual-chamber calorimeter and the electrical method. The calorimeter obtains an outstanding accuracy in measurement of low losses in both inductors.
Figure 4.16 – Electrical $B-I$ measurements for loss evaluation in the ferrite 68 inductor. (a) to (d) present the $B-I$ curves for the ferrite 68 inductor with peak currents from 3 A to 3.59 A. These measurements are performed after the thermal steady-state was reached, as previously presented in Figure 4.14a.

The electrical measurements verify the performance of the calorimeter at a relatively low fundamental excitation frequency of 277 kHz. For this frequency range, the BW of the employed probes were sufficient. Nonetheless, for inductors operating at higher frequencies (i.e. several tens of MHz) and with various current waveforms (e.g. triangular, trapezoidal, etc.), BW limitations of electrical probes and their limited accuracies (especially for current) hinder their utility. For such applications, the proposed calorimeter provides a simple, accurate and cost-effective solution to capture the actual losses.
4.1.8 Conclusion

In this part of the chapter, a closed-type dual-chamber calorimeter with an unprecedented accuracy and measurement range was proposed to measure low levels of power dissipation. The system enabled measurement of losses down to 500 mW. The method reduces the measurement time and avoids further data processing by applying a real-time calibration. The heat is transferred based on convection and conduction, enabling measurement of sensitive losses in various power electronics components regardless of their geometry. Using the same water flow in both chambers enabled the application of very low flow rates without the need for flow meters, resulting in a very high accuracy and low system cost and complexity. Employing more accurate water temperature sensors or using liquids with lower heat capacities would increase the system accuracy. The calorimeter offers accurate efficiency measurements for ultra-efficient converters with power transfer capabilities in range of kilowatts. It also enables more precise loss measurements for various power electronics components, especially in the high-frequency domain, where electrical measurements are prone to inaccurate results, such as for the measurement of...
Figure 4.18 – Comparison between calorimetric and accurate electrical measurements for evaluation of inductor losses at 277 kHz. (a) and (b) compare the electrical and calorimetric results for the ferrite 68 and air-core inductors, respectively. The calorimeter is verified by the electrical measurements. For inductors operating at several tens of MHz, where electrical measurements are not suitable anymore, the calorimeter provides a reliable solution.

Transistor switching losses and losses in HF magnetic components, among others. The application of the calorimeter in component-level loss measurement was demonstrated for comparing HF performance of two different inductors. At a relatively low frequency of 277 kHz, a very good match was obtained between the calorimetric results and electrical measurements, indicating the accuracy of the proposed calorimeter for loss measurements at higher frequencies. For higher frequencies, in which electrical measurements fall short in BW and accuracy, the calorimeter offers a simple and reliable solution.
4.2 Loss Measurement Based on Temperature Mapping

4.2.1 Introduction

In this section, we introduce an accurate loss measurement method based on temperature mapping of the elements in a circuit board. This method takes advantage of a thermal camera for capturing thermographs to evaluate the losses of each component in a circuit at different operating conditions. First, a set of DC calibration tests are performed, with the losses being accurately measured using DC current and DC voltage probes. Finally, by analysing the calibration data, the losses of the circuit components can be accurately determined for various conditions such as HF, VHF and pulsed operation. The main advantage of this method is that the time to reach steady-state is lower compared to the dual-chamber calorimeter introduced at the beginning of the chapter. Furthermore, other than the overall loss value, the method specifies the distribution of losses with their individual values for each of the components, which is of great importance for precise evaluation of losses as well as improvement of cooling and performance of each component.

In Chapter 2, a small-signal $C_{iss}$ versus $V_{GS}$ measurement was proposed to evaluate gate loss in WBG transistors at very high frequencies (see Chapter 2, Subsection 2.2.2). In the following, we apply the temperature mapping method for thermal verification of the small-signal gate losses under soft-switching as a case study. Temperature mapping technique, as it will be presented, not only enables accurate measurement of overall losses, but also determines share of losses for each circuit component. Although evaluation of gate loss is investigated here as a case study, the method is applicable to other scenarios and for different power electronics components.

4.2.2 Setup for Gate Loss Measurement Based on Temperature Mapping

The thermal setup which is designed to verify the proposed small-signal method in Chapter 2, Section 2.2.2 is shown in Figure 4.19a. A Quantum Focus Instruments (QFI) IR microscope with a 512 x 512 pixels array provided thermographs of the circuit boards under operation, with high spatial resolution and accurate emissivity correction. The surface of each test board was coated with black paint to increase the emissivity.

Figure 4.19b shows the circuit board designed for $M_1$ GaN transistor (60 V, 48 A, part number EPC2031). A similar PCB was designed for $M_2$ (650 V, 30 A, part number GS66508T; this is the same as $T_1$ in Chapter 2). LMG1020 gate driver was employed with a 5-V DC supply and PWM signal was provided from a Keysight 33600A waveform generator. To reduce gate-loop inductance and minimize distortion in $V_{GS}$ signal, the driver was placed extremely close to the transistor. For this reason, the high resolution of the IR microscope and its magnification are necessary, especially for components with very small cross sectional area such as the LMG1020 gate driver.

Cutouts surrounded heat sources (i.e. the transistor and its gate driver) to minimize heat leakage and increase measurement sensitivity. Also, nylon stand offs with poor thermal conductivities were used to minimize heat conduction from the sources of power dissipation (i.e. transistor and gate driver) to the surrounding environment.
Figure 4.19 – Setup for calorimetric loss measurement based on temperature mapping. (a) A high-resolution IR camera QFI MWIR-512 extracts the thermograph of the DUT when thermal steady-state is reached. A TPP1000 1-GHz voltage probe measures $V_{GS}$ to verify the gate signal. (b) The evaluation PCB for the GaN transistor $M_1$. Inductance between gate driver and the transistor is minimized, with cutouts surrounding the gate driver and the transistor to avoid heat leakage for higher sensitivities. Also, nylon stand offs with poor thermal conductivities were used to minimize heat conduction from the sources of power dissipation to the surrounding environment.

4.2.3 Thermal Modeling

The transistors were driven with their drain shorted to their source to emulate a ZVS condition, as illustrated in Figure 4.20a. $R_{ON}$ and $R_{OFF}$ are the turn-ON and turn-OFF external gate resistors. We set $R_{ON} = R_{OFF} = 0$ to concentrate the loss only in transistor and gate driver, which simplifies calibration tests and data processing.

The steady-state thermal model of such circuit is shown in Figure 4.20b where $P_{GD}$ and $P_{TR}$ are the portions of gate loss incurred in gate driver and transistor, respectively.
4.2. Loss Measurement Based on Temperature Mapping

![Diagram](image)

**Figure 4.20** – DC calibrations and thermal modelling for M₁ circuit, used to verify the small-signal method for gate loss evaluation in Chapter 2 with the temperature mapping method. (a) Electrical schematic of the setup for measuring $P_G$. For simpler calibration, $R_{ON} = R_{OFF} = 0$. LMG1020 was used to drive M₁ and M₂. (b) Steady-state electrical equivalent of the thermal model for the circuit. (c) DC calibration thermographs of M₁ board when only the transistor dissipates power in reverse-conduction mode and (d) corresponding case temperature at different power levels recorded for the transistor and the gate driver. (e) DC calibration thermographs of M₁ board when only the gate driver dissipates power and (f) corresponding case temperature of the transistor and the gate driver at different power level. A similar calibration was performed for M₂ board.

Two sets of DC calibrations were performed to obtain thermal resistance values of Figure 4.20b. First, the transistor was made the only heat source in the PCB by operating it in its reverse conduction mode (by passing current through its body diode) and the case temperatures ($T_{CASE}$) of the transistor and the gate driver were recorded. Figures 4.20c, 4.20d show the thermographs of this calibration and the extracted case temperatures. Next, the gate drive was made the only heat source in the circuit by shorting its output and...
supplying its input with a DC source. Figures 4.20e, 4.20f show the thermographs of the circuit board as well the recorded $T_{\text{CASE}}$ for the transistor and the gate driver. A similar set of calibrations were performed for the transistor $M_2$.

After performing the calibrations, one can extract the conductance coefficients\(^1\) ($G_{ij}$; $i,j \in \{1,2\}$), which then are going to be used to extract $P_{GD}$ and $P_{TR}$ values as

\[
\begin{bmatrix}
P_{GD} \\
P_{TR}
\end{bmatrix} =
\begin{bmatrix}
G_{11} & G_{12} \\
G_{21} & G_{22}
\end{bmatrix}
\begin{bmatrix}
T_{GD} - T_{\text{amb}} \\
T_{TR} - T_{\text{amb}}
\end{bmatrix}
\]

(4.9)

4.2.4 Verification and Conclusion

$M_1$ and $M_2$ were switched up to 15 MHz and 30 MHz, respectively, and case temperatures of the gate driver ($T_{GD}$) and the transistor ($T_{TR}$), as well as the ambient temperature ($T_{\text{amb}}$) were recorded at steady state for different frequencies. Such an experiment is summarized in Figures 4.21a, 4.21b for $M_1$, as its gate was switched at 15 MHz. Above 15 MHz, the temperatures could exceed the maximum operating temperature for the transistor (150 °C) and the over-temperature protection (shutdown) limit of the gate driver (170 °C).

By using (4.9), the total gate loss is

\[
P_G = P_{GD} + P_{TR}
\]

(4.11)

To further clarify (4.11), we should look into the gate driving circuitry. In the case of hard gating (which is the only driving condition discussed in this thesis), the push-pull transistors within the gate driver are hard switched, as they are driving a capacitive load, the input capacitance of a FET. Therefore, as (4.11) indicates, one needs to sum up the generated heat from the gate driver (as a consequence of hard switching and conduction losses of its internal transistors) and the loss generated inside the transistor due to its inner gate resistance. Adding external gate resistors between the gate driver and the transistor (which is avoided here), changes the distribution of gate loss, as the heat is not generated only from the transistor and the gate driver, but also from the external resistors.

Figures 4.21c, 4.21d present the agreement between the thermal measurement results based on temperature mapping, obtained from (4.9) and (4.11) (discrete points), and the estimated $P_G$ based on small-signal measurements extracted from (2.1) and (2.2) (straight lines). In either case, the accuracy of both methods were verified by direct measurements of input power (DC voltage and DC current) to the gate driver.

\(^1\)An example of such matrix extracted for $M_1$ transistor looks like:

\[
\begin{bmatrix}
G_{11} & G_{12} \\
G_{21} & G_{22}
\end{bmatrix} =
\begin{bmatrix}
0.00122148 & -0.00902151 \\
-0.00902151 & 0.0129189
\end{bmatrix}
\]

(4.10)
4.2. Loss Measurement Based on Temperature Mapping

Figure 4.21 – Extracting gate loss based on temperature mapping method. (a) \(V_{GS}\) applied to \(M_1\) transistor at 15 MHz with turn ON/OFF voltages of 4.9 V/0 V and (b) its corresponding thermograph. The PCB is sprayed with black color to increase emissivity. \(P_G\) versus \(f_{SW}\) for (c) \(M_1\) and (d) \(M_2\). Both transistors were operating between \(V_{ON} = 5\) V and \(V_{OFF} = 0\) V using LMG1020 gate drivers. Thermal results verify the validity of the small-signal electrical method proposed in Chapter 2 for evaluation of \(P_G\).

Loss measurement based on temperature mapping is highly instrumental to the breakdown of losses in various components in a circuit board. Unlike the dual-chamber calorimeter, this method requires DC calibrations and post processing of data to extract the conductance coefficients for each circuit; nonetheless, the steady state in this method is reached within a few minutes, making it extremely useful for loss measurements in HF and VHF circuits.
5 Enhanced Soft-Switching DC-DC Topologies

In Chapter 2, we used novel techniques to quantify the losses for soft-switched WBG semiconductors. Based on the presented comparison, one can optimize the selection of transistors based on parameters such as gate loss, output capacitance loss and conduction loss. Chapter 3 highlighted the importance of designing magnetic components with high qualities and wide BW, and in Chapter 4, we proposed methods to capture the losses and measure system-level as well as component-level efficiency.

This chapter focuses on enhancement of isolated and non-isolated DC-DC converters. To reveal the full potential of GaN and SiC technologies - which translates into designing converters with simultaneously high efficiencies and high power densities - existing topologies and their control strategies has to be enhanced and adapted for HF low-loss operation modes.

The main challenge is to prevent hard switching in quasi-resonant converters at high-frequencies, which otherwise could result in excessive losses and eventually, failure of hard switched transistors. Avoiding hard switching by expansion of soft-switching operation not only increases converter efficiency, but also improves its performance in terms of EMI.

For decades, tap changers have been used in low-frequency (i.e. 50/60 Hz) AC transformers to improve the voltage regulation in AC power systems [111–113]. In power electronics, a DAB converter can be regarded as a DC transformer. In the first part of this chapter, we present an enhanced DAB, or E-DAB topology which is inspired from 50/60-Hz transformers and their tap changers in AC power systems. Optimized for HF operation, the topology significantly improves the efficiency, soft-switching capability, voltage gain ($G$) range and controllability of typical DAB converters by employing a variable-tap HF transformer and a tap changer mechanism. Section 5.1 provides comprehensive analysis with substantial experimental results on the operation and control of the converter.

In the second part of the chapter, a new operation mode for boost converters based on impulse rectification is introduced, which enables their soft-switching operation at high switching frequencies. Section 5.2 encompasses the theoretical analyses of the proposed operational mode, as well as converter design optimization for realizing an ultra-dense boost converter based on WBG technologies and the presented soft-switching scheme.
5.1 Enhanced DAB (E-DAB) Converter

5.1.1 Introduction: A Review of Performance Improvement Methods for DAB Converters

A DAB converter can be regarded as a regulated DC transformer, capable of adjusting its output voltage under varying load and input voltage conditions. It controls the power flow bidirectionally and provides galvanic isolation, which is important for safety and protection. As a consequence, DAB is of great interest for a wide range of applications, including EV chargers, avionics, uninterruptible power supplies, DC micro-grid distribution networks, converters for renewable energy harvesting and telecommunications [96, 114–116].

Power transfer in DAB is inductive, and the series inductance with the employed transformer in a DAB is responsible for power transfer and achieving soft-switching, and by designing transformers with specific turns ratios, the desired voltage step-up/down is achieved. Relying on inductance for power transfer, the large size of magnetic components limits the power density at low switching frequencies; therefore, increasing switching frequency can significantly reduce the overall size of the transformer and its core loss. The same is true of other topologies based on inductive power transfer such as PSFB, LLC, boost etc. [61].

As we discussed in Chapter 2, WBG technology and especially GaN transistors offer smaller $C_{\text{iss}}$ and $R_{\text{DS(on)}}$ compared to their Si counterparts. These unique properties together with the aforementioned advantage of shrinking passive components are highly promising to increase the efficiency and power density of soft-switched topologies such as HF DABs.

Nevertheless, in the case of HF DAB converters, maintaining soft-switching is extremely important. Losing ZVS results in hard-switching losses, and due to being scaled up with frequency, those losses are immense at HF. As a consequence, not only a drastic drop occurs in the efficiency, but also the transistors might experience thermal runaway and eventually fail.

Several methods have been proposed to extend soft-switching in DAB converters. Among them, increasing the dead-time could improve the soft-switching at light loads at the cost of degraded efficiencies at heavy loads; moreover, when the inductor current reaches zero, increasing dead-time does not help at all, leading to more losses [117]. Additionally, real-time adjustment of dead times is not straightforward for HF converters due to all the delays involved in measurements, feedback loops and execution of algorithms [118].

Various modulation schemes can broaden the soft-switching region of a DAB [117, 119–121], but the laborious calculations involved in those methods are difficult to be performed at high switching frequencies mainly because of the limited time resolutions of typical digital PWM controllers, as well as nonidentical propagation delays between different gate drivers (even for those of the same part number).

Another solution is to obtain a resonance to extend the soft-switching region by adding extra passive or active components which are not lossless, add to the design size and complexity [119, 121, 122], and lead to EMI issues as the increased gain depends on a frequency modulation [123].

DC blocking capacitor together with a new modulation scheme is proposed in [124] and the method can
5.1. Enhanced DAB (E-DAB) Converter

successfully increase efficiency for voltage gains around 2 p.u. (twice the nominal gain) but deteriorates the performance under normal operating conditions. The improved performance depends on the proper choice of the blocking capacitor and the \( B-H \) curve of the transformer is prone to shifting, which brings forward the need to deploy an extra saturation prevention algorithm [125].

Combining DAB with elementary buck and boost converters as a composite converter is proposed in [126], achieving outstanding light-load efficiency extension; nonetheless, that comes at the price of losing galvanic isolation and is suited when the difference between input and output voltage levels is relatively small. The increased control complexities make this approach less applicable at high frequencies.

In [127], a planar transformer with two taps is used to successfully extend the soft-switching range and reduce circulating currents in a DAB. However, due to small leakage inductance in the planar transformers [61, 128], an external inductor had to be added in series with the transformer at its high-voltage side, which limited the converter power density, as designing small and efficient HF inductors is challenging [26, 93].

Different tap-changer mechanisms are studied in [129]. Simulation is used to show the advantage of using tap changers for lower semiconductor losses and smaller transformer currents; although measurements at voltage gains equal to the nominal tap value supports the generality of the method, no investigation follows on the superiority of the method at other gain conditions.

In Subsection 5.1.2, we theoretically show the advantage of using an adjustable-tap HF transformer to extend the power-transfer capability and voltage gains under which the proposed E-DAB converter extends ZVS operation. Subsection 5.1.3 presents two different HF transformer geometries: a planar design and a matrix transformer which is realized using Litz wires. Both designs are compared for their \( Q \) factor, leakage inductance (\( L_r \), or namely resonant inductance) and the variation of \( L_r \) with the taps, which is a crucial parameter in designing E-DAB converters. Subsection 5.1.4 focuses on the design of compact GaN-based full bridges, including four-layer PCB layouts for minimized gate and power loops, together with the choice of driving circuitry. In Subsection 5.1.5, the theoretical prediction is verified by various experiments, highlight the importance of the gain versus power-transfer characteristic plane which is proposed to control E-DABs for efficiency maximization. Subsection 5.1.6 discusses the application of E-DAB for efficient charging of lithium-ion (Li-ion) batteries at their different charging phases. Moreover, FEA are conducted for the magnetic flux density and its distribution in the ferrite cores under various load conditions to verify the effectiveness of the proposed E-DAB in efficiency extension at light loads, and the on-load operation of the electromagnetic (EM) relays employed in the tap-changer mechanism is demonstrated. Subsection 5.1.7 concludes the most important aspects of the design and performance of the E-DAB converter.

5.1.2 E-DAB Operation Methodology

Power transfer in DAB converters is inductive and the phase shift between the voltages over the transformer primary and secondary sides, \( \phi \), determines the power transfer in single-phase-shift (SPS) modulation.
Figure 5.1 – E-DAB converter topology and its operational methodology. (a) The converter takes advantage of the transformer leakage inductance and employs a tap changer to increase the power-transfer capability and extend the voltage gains under which the converter is soft switched. Normalized gain versus phase shift is shown for (b) a conventional DAB with a fixed turns ratio of $n$ and (c) an E-DAB with turns ratios adjustable by ±50% from $n$. The shaded areas designate ZVS operation. The range is significantly extended in the case of the E-DAB, especially at light loads.

The performance of the E-DAB converter can be described by the following equation:

\[
P = \frac{V_{IN}V_{OUT}(\phi)(1-\frac{\phi}{\pi})}{2nf_{SW}L_r}
\]  

(5.1)

in which $V_{IN}$ and $V_{OUT}$ are primary and secondary DC-link voltages, respectively, $f_{SW}$ is switching frequency, $L_r$ and $n$ are the leakage inductance and turns ratio of the transformer, respectively. As formulated in (5.1), changing $n$ not only can control the power flow (and hence regulate the voltage), but also is an important parameter determining the soft-switching region, under which the transistors operate with the least stress and power dissipation. To achieve soft-switching, the current through $L_r$ should be large enough to discharge the output capacitance of the switches in the bridges, which means that the
DAB voltage gain, $G$, should stay within definitive constraints of $[117, 130]$

$$n \left(1 - \frac{2\phi}{\pi}\right) < G < \frac{n}{1 - \frac{2\phi}{\pi}} \quad (5.2)$$

Figure 5.1a shows the E-DAB topology. The limits of (5.2) are applied to a DAB with a fixed turns ratio $n$, as illustrated in Figure 5.1b, where the shaded area shows the soft-switching region. Figure 5.1c shows the corresponding ZVS limits for an E-DAB whose turns ratio can be tuned between $0.5n$ and $1.5n$. Theoretically, a broader soft-switching region can be obtained over wider gain ranges, especially at lower phase shifts, the equivalent of light-load operation in which a normal DAB suffers from hard-switching. As (5.1) suggests, the variable turns ratio provides adjustable power-transfer capability for the E-DAB. To that end, designing a tapped HF transformer along with the selection of a tap-changer mechanism are the only requirements to extend soft-switching range and achieve an adjustable power-transfer capability.

### 5.1.3 High-Frequency Variable-Tap Transformers for the E-DAB

A HF transformer provides the required voltage step-up/-down and galvanic isolation, and its leakage inductance – if adequate – enables soft switching. For evaluating the theory presented in Section 5.1.2, we designed tapped transformers with two different geometries; a planar design with PCB traces and a matrix transformer with Litz wires, as presented in Figures 5.2a, 5.2b, respectively.

The planar transformer consisted of E58/11/38 cores from 3C95 ferrite material, two LV primary layers and six high-voltage (HV) secondary layers, as illustrated in Figure 5.2a. The ratio $n$ varied between 3 to 18, with steps of 3. The matrix transformer consisted of four toroidal R22.1×13.7×7.9 cores with N49 ferrite material. We chose Litz wires S1050/AWG42 for the primary windings and S66/AWG42 for its secondary side. The ratio $n$ varied between 9 to 12, with steps of 1. Figure 5.2b presents the matrix transformer together with the EM relays. The tap changer was placed at the HV side of the transformer to reduce the current stress on the EM relays. The bottom sections in Figures 5.2a, 5.2b present the winding arrangements.

We measured the leakage inductance for each of the transformers via short-circuit tests (shorting the secondary windings and measuring from primary side) using a Keysight E4990A impedance analyzer and a 16047E test fixture. As Figure 5.2c shows, the variation of $L_e$ with $n$ is less steep for the matrix design (by a factor of 2.6 times), which better complies with the assumption used in (5.2) regarding the invariant leakage inductance over different turn ratios. $L_e$ in Figure 5.2c is normalized by its value at $n = 9$ for both of the transformers. $L_e$ is about 10 times larger in the matrix design, as shown for different tap values in Figure 5.2d. Also, $L_e$ in the matrix design obtained one order-of-magnitude higher $Q$ (see Figure 5.2d) at the target switching frequency of 300 kHz, making it extremely suitable for efficient HF operation based on what was discussed in Chapter 3 (transformer leakage inductance resembles an air-core inductor, and $Q$ factor measurements can be used to determine their loss.) To obtain the same inductance as that of the matrix transformer, one needs to add an external inductor ($L_{\text{ext}}$) in series with the planar transformer. As Figure 5.2e shows, even adding an extremely high-$Q$ inductor ($Q \approx 1000$), which is highly challenging to design [26, 89, 93], does not offer the same $Q$ factor as that of the $L_e$ in the matrix transformer. Thus, we
Figure 5.2 – Evaluation of HF tapped transformers with different geometries for the E-DAB topology. (a) Planar transformer. (b) Matrix transformer with Litz windings. (c) Normalized $L_r$ versus $n$. The matrix design exhibits 2.6 times less steep variations. (d) $Q$ versus $L_r$ at 300 kHz for different taps. $Q$ and $L_r$ are an order-of-magnitude higher in the matrix transformer. (e) $L_r$ in the planar design is lower than that of the matrix design, and for having an equal inductance, an external series inductor is required. this plot shows the required $Q$ for the $L_{\text{ext}}$. Even adding $L_{\text{ext}}$ with $Q > 1000$ does not increase the overall $Q$ much. (f) $R_{AC}$ over $f_{OSC}$ for different taps in the matrix transformer. Changing taps does not affect $R_{AC}$ at about 300 kHz; thus, changing taps does not incur any extra losses in the E-DAB.
chose the matrix design for realizing an efficient E-DAB converter.

The winding AC resistance, $R_{AC}$, for the matrix transformer is shown in Figure 5.2f for different taps. $R_{AC}$ is low at the target switching frequency (i.e. 300 kHz) and its value does not vary much for different taps, indicating that the variable-tap transformer does not add any extra losses to the converter.

### 5.1.4 E-DAB Converter Design for High Power Density

To enable a HF operation, we opted for high-performance GaN transistors. For the primary side, low-voltage EPC203x ($x \in \{1, 2, 3\}$) family was chosen and the high-voltage GS5560xx ($x \in \{2B, 4B, 6T, 8T\}$) family was selected for the secondary bridge design. In the following, we explain the selection criterion for the primary and secondary transistors from each device family.

By reducing $R_{DS(ON)}$ in transistors of a same family, their output capacitance becomes larger [131]. Therefore, one should address the trade-off between conduction loss and losses due to losing ZVS as a result of an increased output capacitance. DAB is a quasi-resonant converter, and one can use the energy-balance equations for resonances within a period to obtain a selection criterion. Peak energy stored in $L_r$ can be formulated as

$$E_L = \frac{1}{2} L_r I_M^2$$

in which $I_M$ is the peak inductor current. This energy should be large enough to charge and discharge the output capacitance of switches in each full bridge. The required energy to charge or discharge the $C_{OSS}$ between 0 to $V_M$ for each transistor is

$$E_C = \frac{1}{2} C_{OSS}^e V_M^2$$

where $C_{OSS}^e$ is the energy-related output capacitance of the transistor. Transistors in each of the primary or secondary bridges can be modeled with their energy-related output capacitances at the resonance event. During each resonance, two such capacitors get charged and two get discharged. $C_{PRIMARY}$ and $C_{SECONDARY}$ represent the equivalent capacitances of each bridge at primary and secondary sides, respectively.

By comparing the energy values from (5.3) and (5.4), one can estimate the minimum inductor current (and equivalently power) at which a transistor can be soft-switched in primary and secondary full-bridges. LV EPC transistor (EPC2031, EPC2032 and EPC2033) are compared in Figure 5.3a for their output capacitance versus the minimum required primary current ($I_{PRIMARY}$) for soft-switching. For current values above 3 A, all the three transistors can achieve ZVS. As the converter is high power and the nominal $I_{PRIMARY}$ is in the range of 10 A, we decided to select the EPC2031 with the lowest $R_{DS(ON)}$ to reduce conduction loss, while maintaining ZVS for a broad range, as the transistor is also suitable for light-load operations down to $\approx 3$ A. A similar comparison was performed for HV transistors from GaN Systems, as...
Figure 5.3 – GaN transistor selection criterion for the E-DAB converter. $C_{\text{er OSS}}$ of each transistor is plotted against the minimum required current to achieve ZVS for that specific $C_{\text{er OSS}}$ value. Shaded areas indicate ZVS operation for the selected transistors. (a) For selecting LV transistors, since nominal $I_{\text{PRIMARY}}$ is in the range of 10 A, all the evaluated EPC transistors can achieve ZVS for a large load range. However, EPC2031 was selected, as it enables the lowest conduction loss. (b) GS66502B was selected for having the lowest $C_{\text{er OSS}}$, which reduces secondary-side switching loss at light loads.

shown in Figure 5.3b. The nominal current of the secondary side ($I_{\text{SECONDARY}}$) is in the order of 1 A. Devices with extremely low $R_{\text{DS(ON)}}$ (such as GS66508T) cannot maintain soft switching at light loads. Therefore, we selected the GS66502B transistor with the lowest $C_{\text{OSS}}$ to preserve ZVS at light loads down to $\approx 0.4$ A.

The primary and secondary full bridges based on EPC2031 (60 V, 48 A) and GS66502B (650 V, 7.5 A) are presented in Figures 5.4a, 5.4b) [52].

SI8271 gate drivers provided isolation between the power and control stages with high transient ($dv/dt$) immunities. The PWM signals were generated using a TMS320F28379D controller and were transmitted to the gate drivers by shielded MMCX cables and connectors. To supply the gate drivers, we chose compact isolated DC-DC converters (ADUM5000) capable of withstanding up to 2.5 kV. They were mounted on the bottom layer and provided a 5-V supply for driving of the GaN transistors. Figure 5.4c presents the optimized E-DAB converter with an overall size of $80 \times 50 \times 25$ mm$^3$.

The tap-changer mechanism consists of four EM relays, each capable of switching about 2 A. They were rated for more than 60 VA of apparent power, appropriate for operation at the secondary-side of the E-DAB.

To minimize the gate-loop and power-loop inductances, we designed four-layer PCBs as illustrated in Figure 5.5 for the primary-side full bridge. To the same end, we used multi-layer ceramic capacitors very close to the DC links and gate-driver supplies. A similar high-density design was realized for the secondary-side full bridge. The copper thickness for each of the inner and outer layers was 1 oz (or $\approx 35$ µm).
Figure 5.4 – The E-DAB converter consists of GaN transistors, a high-frequency tapped transformer and its tap-changer mechanism. (a) Primary full bridge at LV side with EPC2031 transistors. (b) Secondary full bridge at HV side employing GS66502B transistors. (c) The final E-DAB converter with a compact design.

In order to make an experimental comparison between the performance and efficiency of the E-DAB and the DAB without the risk of device thermal runaway, forced-air cooling was used at various conditions, especially at the limit of transition from ZVS to hard switching, whereby the transistors were exposed to high levels of switching losses.
5.1.5 Experimental Results and Performance Verification

Using SPS modulation, square-wave voltages on the transformer primary ($V_{\text{PRIMARY}}$) and secondary ($V_{\text{SECONDARY}}$) were generated, as shown in Figure 5.6. The output voltage of the converter was regulated at 400V by changing $\phi$ and $n$ at a constant load. Under these conditions, the efficiency of the E-DAB for different tap values was measured for different input powers (Figure 5.7) while the input voltage was matched with the nominal gain of each tap, i.e. output voltage divided by $n$. The input voltage at which the converter could still operate efficiently (with full or partial ZVS) could be significantly extended by tuning the turns ratio. Furthermore, when a high power-transfer was required and even maximizing $\phi$ cannot be sufficient to reach the required target power, changing $n$ increases the power-transfer capability.
5.1. Enhanced DAB (E-DAB) Converter

![Voltage waveforms](image)

Figure 5.6 – Voltage waveforms at primary ($v_{PRI}$) and secondary ($v_{SEC}$) of the HF matrix transformer in the E-DAB operating with SPS modulation at 300 kHz. Adjusting $\phi$ determines the level of the transferred power as well as its direction.

of the converter, as indicated by (5.1).

To verify the extension of soft switching to higher voltage gains as predicted by (5.2), we supplied a relatively light load of 200 W at an output voltage of 400 V with the E-DAB and a conventional DAB. The conventional DAB was realized by using the fixed tap of $n = 10$ in the E-DAB for all the experiments.

![Efficiency curve](image)

Figure 5.7 – E-DAB efficiency versus input power for different taps at a fixed output voltage of 400 V and at gains equal to $n$. Adjusting $n$ not only helps to increase the power capability when the phase shift reaches its maximum limit, i.e. 90°, but also increases the efficiency at light and heavy loads.
Figure 5.8 compares the efficiency of the E-DAB and the DAB converters, where the E-DAB outperforms the conventional DAB for the entire input voltage range, the equivalent of up to 2.8 times higher voltage gains compared to the DAB. In addition, the peak efficiency was increased from 96.5% to 97.4%. The subsequent reduction in the losses significantly reduces the risk of thermal runaway and device failure, particularly at light loads and wide-gain operations.

Figures 5.9a, 5.10a compare primary-side transformer voltage waveforms, $v_{PRI}$, for DAB and E-DAB converters as both were operated at 200 W. They represent the operation of the converters at three different gain values, corresponding to the dashed lines in Figure 5.8.

To observe the switching behavior of the GaN transistors, we have measured gate-to-source voltage, $v_{GS}$, and drain-to-source voltage, $v_{DS}$, of the two low-side primary transistors using Tektronix TPP1000 1-GHz voltage probes for turn-OFF (Figures 5.9b, 5.10b) and turn-ON (Figures 5.9c, 5.10c) transients. Higher gains result in lower efficiencies in the DAB, whereas the E-DAB achieves higher efficiencies as predicted by (5.2) by avoiding a hard switching.

Figures 5.11a-5.11c show the amplitude spectrum of $v_{PRI}$ over frequency for both converters at $G = 11.8$, 13.9 and 17.8, respectively. Hard switching in the conventional DAB at higher gain values not only results in lower efficiencies, but also generates harmonics at frequencies between 10 MHz to 200 MHz, which can lead to EMI issues in the converter. For instance, the $v_{GS}$ waveforms of the DAB in Figure 5.9c suffer from relatively larger oscillations compared to those for the E-DAB, shown in Figure 5.10c. Such EMI issues can cause false triggering and device failure, especially in GaN devices with low turn-ON
5.1. Enhanced DAB (E-DAB) Converter

Figure 5.9 – Transistor switching behavior in the DAB converter at 200 W and for $G = 11.8$, 13.9 and 17.8. (a) Transformer $v_{PRI}$ with the corresponding efficiencies. The $v_{GS}$ and $v_{DS}$ waveforms for (b) turn-OFF and (c) turn-ON transients of the two low-side primary switches. By increasing $G$, the partial ZVS behavior for turn-ON transient changes into hard switching and even reverse conduction of the high-side device, leading to higher switching losses.
Figure 5.10 – Transistor switching behavior in the E-DAB converter at 200 W and for $G = 11.8$, 13.9 and 17.8. (a) Transformer $v_{PRI}$ with the corresponding efficiencies. The $v_{GS}$ and $v_{DS}$ waveforms are shown for (b) turn-OFF and (c) turn-ON transients of the two low-side primary switches. By increasing $G$, the full ZVS behavior for turn-ON transient changes into a partial ZVS; avoiding a hard switching leads to higher efficiencies compared to the DAB at the same operating conditions.
5.1. Enhanced DAB (E-DAB) Converter

Figure 5.11 – Single-sided amplitude spectrum of $v_{PRI}(t)$ from 10 MHz to 200 MHz, compared for the DAB and the E-DAB for $G$ values of (a) 11.8, (b) 13.9 and (c) 17.8, corresponding to the waveforms presented in Figures 5.9a, 5.10a. Extended ZVS in the E-DAB topology results in significantly lower amplitudes of high-frequency harmonics and thus higher overall efficiencies.
thresholds and small gate breakdown voltages.

For a fixed output voltage, one can solve the limits for $G$ as indicated by (5.2) for different values of $\phi$ and use (5.1) to obtain a gain versus power-transfer characteristic plane for the E-DAB. Combined with the power-transfer limit due to the maximum $\phi$, such a characteristic specifies the operating range in which the E-DAB is soft switched for its different $n$ values. The characteristic plane is presented in Figure 5.12a for the E-DAB converter operating at a 400-V fixed output voltage [6]. We experimentally verified the analysis by comparing the E-DAB with the DAB at a fixed voltage gain of 15.5. As compared in Figure 5.12b, the E-DAB preserved higher efficiencies compared to the DAB over the entire power sweep and increased the efficiency by 5% at an extremely light load of 80 W. Moreover, when phase shift reached its maximum value in the DAB (i.e. 90 degrees), the E-DAB could still transfer more power. The aforementioned power-transfer limit for the DAB is indicated by the shaded area in Figure 5.12b.

The gain versus power-transfer characteristic is an important analysis tool for sizing, design, and control of E-DAB converters. Taps for HF transformers can be selected based on gain and power requirements of the target application. Besides, a controller can maximize the efficiency of the E-DAB based on the presented characteristics plane by selecting proper values for $\phi$ and $n$ at any given operating condition, so that always ZVS is preserved.
5.1. Enhanced DAB (E-DAB) Converter

Figure 5.12 – Gain versus power-transfer characteristics of the E-DAB converter used for analysis of efficiency over different voltage gains and power levels. (a) Gain versus power-transfer characteristics of the E-DAB converter. The shaded areas indicate ZVS operation of the E-DAB for different taps. (b) Experimental evaluation of efficiency versus power at a fixed 400-V output voltage and $G = 15.5$. The shaded area indicates the power-transfer limit of the DAB. Experimental results verify the theoretical prediction of the gain versus power-transfer characteristics plane, as the E-DAB could always outperform the DAB in terms of efficiency.
Chapter 5. Enhanced Soft-Switching DC-DC Topologies

5.1.6 Discussion

Here, we demonstrate the superiority of the E-DAB topology over a conventional DAB for efficient charging of Li-ion batteries based on their specific charging profiles. Next, we address important operational aspects of the E-DAB converter, including the variation of transformer core losses at different load conditions and the dynamics of the tap changer.

Application of E-DAB in Ultra-Efficient Li-Ion Battery Charging

Li-ion batteries are rechargeable and commonly used in portable electronics, EVs and aerospace applications. A Li-ion battery is charged in two stages: constant current (CC) and constant voltage (CV). During the CC phase, the charger applies a constant current to the battery when its voltage is increasing steadily. Next, in the CV phase, the voltage is kept constant and the current gradually declines towards zero, and charging is completed after a certain minimum threshold for the current is hit.

Figure 5.13 illustrates the gain versus power-transfer characteristic plane for the E-DAB with the two charging phases (i.e. CC and CV). In this case, the E-DAB can charge a Li-ion battery in step-down mode, when the power is supplied from the HV side at 400 V to the LV Li-ion batteries (the charging profile of a single-cell Li-ion battery is scaled up in voltage and current). In the CC phase, the battery is being charged and its voltage is increasing gradually. Thus, the gain is reducing while the power increases. The E-DAB can preserve its ZVS behavior by shifting the taps to lower values and continues to charge with a high efficiency over the entire charging process.

Figure 5.13 – Application of the E-DAB converter in ultra-efficient Li-ion battery charging. By tuning the tap values, E-DAB can maintain soft switching over the entire CC and CV charging phases.
5.1. Enhanced DAB (E-DAB) Converter

Transformer Core Loss at Light-Load Conditions

It was shown in Figures 5.12a, 5.12b that for a fixed voltage gain, E-DAB achieved higher efficiencies over the entire power range. We related this superior performance to the extended soft-switching range for the E-DAB. Now, it is worth investigating transformer core loss as a potential limiting factor for maintaining a high efficiency at light loads.

We used FEA simulations to obtain the distribution and amplitude of $B$ inside the matrix transformer cores at different loading conditions to compare the core losses. Higher $B$ results in an increased core loss. Figure 5.14 presents the FEA results when the matrix transformer was subjected to a 40-V 300-kHz sine voltage excitation at its primary side when different load resistances ($R_L$) were placed at its secondary side. After a certain reduction in the load (or a certain increase of $R_L$), the transformer operates similar to a no-load condition with highest core loss (as there is almost no flux cancellation occurring in the core). The increase of $B$ remains negligible between 20%, 10% and 5% of full load.

Despite the absence of flux cancellation at light loads, the proper sizing of the transformer cores enabled

![Figure 5.14](image)

**Figure 5.14 – FEA results for magnitude and distribution of $B$ in the HF transformer cores under different load conditions at a 40-V 300-kHz voltage excitation at the primary side of the transformer. After a certain increase in $R_L$, $B$ does not increase any further and remains almost similar for 20%, 10% and 5% of the full load. Thus, core loss does not increase drastically and is not a bottleneck for efficiency even at extremely light loads.**
achieving low levels of core loss, which could otherwise limit the efficiency at light loads even by choosing the best tap value of the E-DAB. This enabled high efficiencies without sacrificing the converter size and volume, as a high power density of 10 kW/l (or 164 W/inch\(^3\)) together with a peak efficiency of 97.4% were simultaneously achieved.

**Operation of the Tap Changer**

EM relays can be actuated under different load conditions as they are able to conduct and block current in both directions [132]. The switching transient of the employed EM relays is shown in Figures 5.15a, 5.15b for an operation under 28 V and 2.8 A. As presented in Figure 5.15a, it takes about 20 ms for the coil in the EM relay to be charged (the blue curve) and then the contact is activated (the red curve). Figure 5.15b shows a contact switching time of < 5 ns. In fact, the delay for the activation of the EM relays is much smaller than system-level dynamics in typical applications in which E-DAB converters operate, such as: photovoltaics (PV) energy harvesting with slow variations of temperature and solar irradiance over time, or Li-ion battery charging when a full charging cycle lasts for several minutes and battery voltage varies slowly over time.

For increasing the lifetime of EM relays, Off-load tap changing is recommended; however, the EM relays are also capable of on-load operation. Figures 5.15c, 5.15d show the variation of the HV DC-link voltage for on-load opening and closing transients, respectively, and their insets provide a finer time scale of the DC-link voltage and \(v_{DS}\) for a secondary-side transistor.

The behavior of the converter is determined by the characteristics of the DC link, including its resistance (load) and capacitance.

The taps were placed at the HV side of the matrix transformer in order to minimize current stress on the EM relays. Off-load tap changing increases the lifetime of the EM relays. Also, for a better lifetime with a faster activation time, one can employ solid-state switches in the tap-changer mechanism; however, the efficiency might be slightly lower than the case in which EM relays are used [129].
Figure 5.15 – Evaluation of EM relays for their transient performance. (a) ms-scale coil charging transient (blue curve) and contact voltage waveform (red curve). (b) ns-scale switching transient of the EM relay. The EM relays provide ns-range switching after an activation delay of \( \approx 20 \) ms. (c) Opening and (d) closing transients with variation of the output DC-link voltage. The insets on the right provide a finer time-scale for \( v_{\text{DC}} \) and \( v_{\text{DS}} \) of a secondary low-side transistor.
5.1.7 Conclusion

In this part of the chapter, a method to enhance the performance of HF isolated DC-DC converters was introduced. Next, we presented a full assessment of the proposed enhanced DAB (or E-DAB) converter, which by utilizing an adjustable-tap HF matrix transformer, increases power-transfer capability and extends soft-switching range over higher voltage gains compared to a conventional DAB. Two different transformer geometries were designed and compared for the amount and quality factor of their leakage inductances, where a matrix design with Litz wires exhibited a superior performance compared to the planar design with PCB traces. By employing the matrix transformer equipped with an electromagnetic tap changer, and by using the simplest modulation technique (i.e. SPS), the E-DAB converter achieved a peak efficiency of 97.4% with an overall efficiency always greater than that of a conventional DAB for up to 2.8 times higher voltage gains even under light-load conditions.

Experimental results were presented, where the analysis of switching transients and amplitude spectrum proved the effectiveness of using the turns ratio for minimizing the losses in the HF E-DAB converter. Finite-element analysis of magnetic flux density in the ferrite cores were used to investigate light-load core loss, and by the proper sizing of the transformer, low core loss and a high power density of 10 kW/l (or 164 W/inch$^3$) were achieved.

We proposed a gain versus power-transfer characteristic plane which is of great importance to the design and control of E-DAB converters. We further demonstrated the compact design of GaN-based full bridges including the details on HF PCB layout and driving stages. The transient behavior of the tap-changer mechanism was analyzed with two examples of on-load operation.

The E-DAB topology provides superior performance in terms of flexibility, regulation capability and efficiency with applications in ultra-efficient Li-ion battery charging, renewable energy harvesting and DC voltage transformation in future DC distribution systems, among others. Thanks to the extended ZVS, E-DABs based on SiC and GaN transistors can operate at high frequencies with the added benefit of reduced volume and weight.
5.2 Optimized Boost Converter Based on Impulse Rectification

5.2.1 Introduction

Boost converters are main building blocks in power electronics and are used in a wide range of voltage step-up applications. In a conventional boost converter at continuous conduction mode (CCM), the transistor is subjected to hard switching, which hinders an efficient power conversion, especially at high and very-high frequencies.

In this part of the chapter, we first present an operation mode for boost converters which enables soft-switching based on rectification of repetitive impulses, which was initially recommended by Samizadeh et al. for high step-up DC-DC conversion [55]. Thanks to providing ZVS for the transistor, the impulse rectification mode enables efficient HF operation of WBG devices and small inductor volumes.

Next, to achieve a simultaneously high efficiency and high power density, an optimum PCB layout with outstanding cooling capability is designed. Based on the guidelines presented in Chapter 3, several inductors are compared to realize a high-current wide-BW inductance. The effect of different inductor geometries and windings on the converter efficiency is comprehensively investigated. Furthermore, the choice of rectifier devices and their current rating impact on the overall conversion efficiency are discussed thoroughly. A novel control strategy is then proposed to ensure ZVS and therefore guarantee a safe and efficient operation of the converter over different voltage gains and load conditions.

Finally, an insightful loss breakdown of the boost converter based on the measurement methods presented in the previous chapters is given, quantifying the losses down to the level of transistor loss sub-components. Subsequently, the efficiency and power density of the converters presented in this thesis are benchmarked against state-of-the-art DC-DC converters, showing the superiority of the proposed converters.

5.2.2 Operation Principle

A typical boost converter can be regarded as a combination of impulse generator and impulse rectifier networks, as presented in Figure 5.16. The impulse generator circuit consists of the inductor $L$ in series with the FET (and its output capacitance, $C_{OSS}$). The impulse rectifier stage includes a diode rectifier connected to an output DC-link capacitor.

![Figure 5.16 – Boost converters can be operated in impulse rectification mode with ZVS, without adding any extra hardware. The impulse generator and impulse rectifier networks are separately highlighted.](image-url)
Figure 5.17 demonstrates the detailed operation of the boost converter in impulse rectification mode for different time intervals within a switching period. From $t_0$ to $t_1$, the FET is turned ON and the inductor is charged with the input voltage source, $V_{IN}$, up to a maximum current of $I_M$. At $t_1$, the FET is turned OFF. The interruption of current through transistor channel results in the formation of an $LC$ resonance between $L$ and $C_{OSS}$. Typically the turn-OFF duration of the transistor is much faster than the $\sqrt{LC_{OSS}}$ time constant, which results in zero losses during the turn OFF. In the absence of an impulse rectifier stage, an impulse with a large amplitude is formed, as the dashed curve in Figure 5.17 illustrates. Nonetheless, in presence of the impulse rectifier stage and an output DC-link voltage of $V_{OUT}$, the $v_{DS}$ gets clamped to $V_{OUT}$. This phase starts at $t_2$, through which the power is transferred to the output until $t_3$. At this moment, the inductor current reaches zero, and the power transfer to the output is ended. Between $t_3$ and $t_4$, the energy from $C_{OSS}$ is restored in $L$, resulting in a negative inductor current and drop of $v_{DS}$ to zero. Right after $t_4$, a new period is started, and the transistor is turned ON when its $v_{DS}$ is still zero, which provides a ZVS operation.

For simplicity, we neglect the transistor losses described in Chapter 2 to extract the amplitude of the generated impulse voltage, $V_M$, as

$$V_M = Z I_M$$

in which

$$Z = \sqrt{\frac{L}{C_{er_{OSS}}}}$$

$C_{er_{OSS}}$ in (5.6) is the energy-related output capacitance of the transistor, which by definition is the capacitance that provides the same stored energy as that of the transistor output capacitance when $v_{DS}$ rises from zero to $V_M$.

The inductor peak current, $I_M$ can be formulated as

$$I_M = \frac{V_{IN} T_{ON}}{L}$$

$T_{ON}$ is the FET ON time or the inductor charging time, which is equal to the interval between $t_0$ to $t_1$. As mentioned in Chapter 3, the inductor resistance components are $R_C$ and $R_{AC}$. Then the inductor charging time constant can be formulated as

$$\tau = \frac{L}{R_C + R_{AC}}.$$
5.2. Optimized Boost Converter Based on Impulse Rectification

Figure 5.17 – Waveforms illustrating the operation of the boost converter based on impulse rectification mode for different time intervals within a switching period. After the transistor is turned OFF, \( v_{DS} \), which would otherwise appear as a high-amplitude impulse, gets clamped to the output DC-link voltage. The resulted ZVS in this operation mode is highly favorable to HF power conversion.

In a no-load operation, \( V_{OUT} = V_M \) and when the converter is providing a power to the output, \( V_{OUT} < V_M \). Therefore, one can define the maximum converter gain (\( G_{MAX} \)) as

\[
G_{MAX} = \frac{V_M}{V_{IN}} \tag{5.9}
\]

By supposing \( T_{ON} = \tau \) and utilizing (5.5) and (5.7), we derive

\[
G_{MAX} = \frac{Z}{R_C + R_{AC}} \tag{5.10}
\]
Chapter 5. Enhanced Soft-Switching DC-DC Topologies

At each switching period, the energy transferred to the output, $E_{OUT}$, can be equated as

$$E_{OUT} = \frac{1}{2} L I_M^2 - \frac{1}{2} C_{OSS} V_{OUT}^2$$

(5.11)

By using (5.5) and (5.6), one can rewrite (5.11) as

$$E_{OUT} = \frac{1}{2} C_{OSS} (V_M^2 - V_{OUT}^2)$$

(5.12)

We can formulate (5.12) based on $V_{IN}$ and voltage gains only, by considering $V_M = G_{MAX} V_{IN}$ and $V_{OUT} = M V_{IN}$ ($G$ is the actual voltage gain in the presence of a load at DC-link voltage of $V_{OUT}$), as

$$E_{OUT} = \frac{1}{2} C_{OSS} V_{IN}^2 (G_{MAX}^2 - G^2)$$

(5.13)

The transferred power can be derived as

$$P_{OUT} = [1 - (\frac{G}{G_{MAX}})^2] P_{MAX}$$

(5.14)

in which

$$P_{MAX} = \frac{1}{2} L I_M^2 f_{SW}$$

(5.15)

From (5.11)-(5.15), one can conclude that for an efficient power transfer, $G_{MAX}$ has to be much greater than $G$. In other words, when $G_{MAX} >> G$, the reactive power in the converter is minimized and more active power is transferred to the output.

Furthermore, by using (5.7) and assuming $T_{ON} \approx 1/f_{SW}$, $P_{MAX}$ can be formulated as

$$P_{MAX} = \frac{V_{IN}^2}{2 L f_{SW}}$$

(5.16)

which shows that the power transfer in the boost converter based on impulse rectification is inversely proportional to the switching frequency. Thus, $f_{SW}$ can be used to regulate the boost power transfer at any specific voltage gain.
5.2. Optimized Boost Converter Based on Impulse Rectification

![Waveform Diagrams]

Figure 5.18 – Comparison of inductor current waveforms for CCM, DCM and impulse rectification in a boost converter. Boost converters are typically operated in CCM and DCM. In the impulse rectification mode, unlike the CCM, the transistor is soft switched, and on the contrary to the DCM, the inductor current does not keep staying at zero for a finite interval.

To clarify the unique operation of boost converters based on impulse rectification, one should consider the inductor current waveform. As Figure 5.18 illustrates, in CCM (top waveform), the current is triangular and non-zero over the entire period. In discontinuous conduction mode (DCM) (the middle waveform), the inductor current hits zero and keeps this value until the beginning of the next switching cycle. Unlike in CCM, the inductor in boost converters based on impulsed rectification mode hits zero twice per switching cycle, which in turn results in soft-switching operation of the converter. Furthermore, unlike DCM, there are no periods during which the inductor current stays zero.

5.2.3 Layout Optimization for an Ultrahigh Power Density

The main challenges for realizing an ultrahigh density converter are an efficient thermal interface design and reduced HF losses [133]. To obtain an efficient thermal interface, the entire power stage was implemented on a single-layer insulated metal substrate (IMS) PCB, as shown in Figure 5.19a.

IMS technology is known for its outstanding thermal performance in high-power LEDs and high-speed motor drives [134, 135].
Figure 5.19b presents the full converter design including a HF inductor along with the IMS PCB layout composed of a 35-µm copper layer, a 50-µm VT4B5 insulation material and a 1-mm aluminum substrate. The overall thermal conductivity \( k_t \) over the entire PCB thickness \( L_t \) is

\[
k_t = \frac{L_t}{\frac{L_1}{k_1} + \frac{L_2}{k_2} + \frac{L_3}{k_3}}
\]

in which \( k_1 = 385 \text{ W/m-K} \), \( k_2 = 4.2 \text{ W/m-K} \) and \( k_3 = 205 \text{ W/m-K} \) represent thermal conductivities of copper, VT4B5 insulation material and aluminum, respectively, and \( L_1 \) to \( L_3 \) are the corresponding...
5.2. Optimized Boost Converter Based on Impulse Rectification

Figure 5.20 – Boost converter waveforms at 1.6 MHz and 40.9% duty cycle when an air-core inductor with 675-strand Litz wire and an 8-A SiC Schottky diode were used. (a) Experimental $v_{DS}$ and $v_{GS}$ waveforms measured with 1-GHz TPP1000 Tektronix voltage probes. (b) $i_L$ and $i_{DS}$ waveforms extracted from a spice simulation (to avoid any disturbances on the circuit operation, we decided not to measure current directly). The converter operated at 430 W of input power and 400 V of output voltage, at $G = 2.3$. By adjusting the $D$, full ZVS was achieved, enabling very high efficiencies at MHz frequencies.

thicknesses of each layer. Using (5.17), the IMS PCB offers $k_t > 60$ W/m-K. Considering the board cross sectional area, an overall thermal resistance of $< 0.02$ K/W was obtained, which is much lower than the junction-to-case thermal resistance of the transistor ($0.5$ K/W for GS66508B) and the diode ($\sim 1$ K/W for IDDD08G65C6), granting a very efficient heat extraction from the devices.

Also for a better inductor cooling, one can employ high thermally conductive epoxies in the so-called pottting process, which are widely used for improving the thermal performance of electrical machines, transformers, inductors, and transistor packages [136–139]. These materials fill the space between the windings and the IMS board and can provide up to two orders of magnitude higher thermal conductivities compared to air.
Additionally, achieving ZVS results in significantly reduced losses by eliminating hard switching. To further improve the efficiency, the GaN device GS66508B, with the lowest soft-switching losses (based on the measurements in Chapter 2), was selected. Figure 5.20a presents $v_{GS}$ and $v_{DS}$ waveforms when the boost converter was fully soft switched at 1.6 MHz, with a 400-V DC output voltage and at a voltage gain of $G = 2.3$. Inductor current ($i_L$) and drain-to-source current ($i_{DS}$) from spice simulation are shown in Figure 5.20b for the same operating conditions. To avoid any disturbances on the circuit operation, we did not measure current waveforms directly.

5.2.4 Wide-Bandwidth Inductor Design and Optimization

Power in a boost converter in impulse rectification mode is regulated by switching frequency. Therefore, to preserve a high efficiency over the entire load range, designing a wide-bandwidth inductor with a high $Q$ is essential.

To optimize the inductor geometry and its material, we designed spiral and toroidal inductors of comparable volumes, with the same type of Litz wire ($S675/AWG48$), as listed in Table 5.1.

As it was discussed in Chapter 3, small-signal $Q$ measurement is highly instrumental to the performance evaluation of air-core inductors. For inductors with a core, this method only takes into account the winding and eddy-current losses; thus, this measurement can be used to evaluate MnZn inductors for their eddy-current losses (the reason for that is the high share of eddy-current loss in MnZn ferrites due to their relatively lower $\rho_c$ values compared to the NiZn ferrites). To extract the BW of the inductors listed in Table 5.1, small-signal $Q$ factor measurements were performed, as shown in Figure 5.21.

It was shown in Chapter 4 that the overall large-signal losses can be accurately measured using the dual-chamber calorimeter. With that background, the small-signal $Q$ measurements presented in Figure 5.21 provide the following information:

The ferrite 68 material exhibits the highest $Q$; however, due to a relatively large magnetic $H_c$ special to NiZn materials, the $Q$ drops drastically at high currents [89, 93] (see Chapter 4). N49 and N87 MnZn ferrites operate efficiently (with $Q > 100$) only for a very limited frequency range and are not suitable for designing efficient wide-BW inductors. With the same overall size, air-core inductors present the widest BW upon which $Q > 100$. Although the spiral inductor has higher $Q$ than its toroidal counterpart, its magnetic field is not confined and its $Q$ is prone to substantial degradation in the vicinity of metallic objects (e.g. PCBs, cold plates etc.). Therefore, we opted for the air-core toroidal design, presented in Figure 5.22a.

<table>
<thead>
<tr>
<th>Geometry</th>
<th>Core Material</th>
<th>Limitation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spiral</td>
<td>Air</td>
<td>Magnetic field is not confined</td>
</tr>
<tr>
<td>Toroidal</td>
<td>Air</td>
<td>Maximum achievable $Q$ is limited</td>
</tr>
<tr>
<td>Toroidal</td>
<td>NiZn (Fair Rite: 68)</td>
<td>$H_c$ is large, only good at low currents</td>
</tr>
<tr>
<td>Toroidal</td>
<td>MnZn (TDK: N49, N87)</td>
<td>$Q$ is not broad over frequency</td>
</tr>
</tbody>
</table>

Table 5.1 – Comparison of inductor geometries and core materials for realizing a high-BW inductor
5.2. Optimized Boost Converter Based on Impulse Rectification

Figure 5.21 – Small-signal Q measurements for different inductor geometries and various HF materials (listed in Table 5.1), using an E4990A Keysight impedance analyzer. All the inductance values are close to 7 µH. MnZn ferrites with N49 and N87 cores suffer from drop of Q at high frequencies, and thus are not suitable for designing wide-BW inductors. The inductor based on 68 NiZn ferrite material obtains the highest small-signal Q; however, due to a large $H_C$, its large-signal Q factor is very low, resulting in large HF losses, especially for high current ratings, as it was measured thermally in Chapter 4. Therefore, an air-core design was selected for the optimum wide-BW and high-current inductor. Toroidal air-core inductors are preferred over the spiral counterparts, as they have a confined magnetic field. This is important especially if the inductor is operated in the proximity of materials with losses at HF, such as aluminum (in the IMS PCB) or FR-4 PCB insulators.

In Chapter 3, the loss in air-core inductors was attributed to winding conductive and proximity-effect resistances, namely $R_{COND}$ and $R_{PROX}$. Based on the theory proposed by Carretero et. al. [140], $R_{COND}$ is inversely proportional to the number of strands, whereas $R_{PROX}$ scales linearly with the strand number. Additionally, $R_{COND}$ affects Q in the low-frequency ranges, whilst $R_{PROX}$ is dominant at high frequencies. Thus, for a fixed inductance value, one can change the strand number to tune the inductor Q and BW. This has been done for three different Litz wires, as shown in Figure 5.22b. The measurements of this plot indicate that by increasing the number of strands in the Litz winding from 180 to 1100, the peak of Q factor increases, while its BW decreases.

In Figures 5.22c and 5.22d, the efficiency, $\eta$, is plotted versus input power, $P_{IN}$, and $f_{SW}$ for $G = 10$ and $G = 4$, respectively. It can be seen that $\eta$ has a strong dependence on the inductor Q factor. The inductor with 1100 strands (S1100) has the highest efficiency at $f_{SW} < 0.5$ MHz (cf. Figures 5.22b, 5.22c). Nonetheless, for $f_{SW} > 2$ MHz, the 180-strand design (S180) has the highest Q and thus the highest $\eta$ (cf. Figures 5.22b, 5.22d). The impact of inductor Q factor on $\eta$ becomes more pronounced at higher G values (cf. Figures 5.22c, 5.22d), whereas for low gains and high powers, the 675-strand design (S675) enables efficiencies similar to that of the 1100-strand design (S1100), as shown in Figure 5.22d, but at a lower cost. For optimizing other circuit parameters, the S675 inductor, which had the highest Q factor between 1 MHz to 2 MHz, was chosen.
Figure 5.22 – Air-core inductor $Q$ factor optimization via choosing different Litz wires, and its consequent effect on the boost converter efficiency. (a) Toroidal air-core inductor with (b) small-signal $Q$ measurements for various AWG48 Litz wires with strand numbers of 180, 675 and 1100. Converter efficiency is plotted versus the input power and switching frequency for voltage gains of (c) $G = 10$ and (d) $G = 4$. The small-signal $Q$ factor of the inductors significantly affects the efficiency, especially at higher voltage gains.
5.2. Optimized Boost Converter Based on Impulse Rectification

5.2.5 Choice of the Rectifier Stage

Zero reverse recovery in SiC Schottky diodes makes them great candidates for HF operation in the boost converter based on impulse rectification. Although synchronous rectification can potentially reduce the conduction losses, it increases complexities in layout design and control (having only a few circuit elements enabled the realization of the entire power stage on a single-layer PCB).

Thus, to be able to optimize the efficiency with diode rectifiers, it is important to quantify the effect of device parameters on the overall $\eta$. Figure 5.23a presents the junction capacitance ($C_J$) against rated current for diodes with different current ratings (from a similar device family). $C_J$ scales linearly with the current and higher $C_J$ result in an increasing in the reactive power; nonetheless, at the same time, device resistance and forward voltage drop decrease. For evaluating the effect of aforementioned parameters on the converter efficiency, converters with 4-A, 8-A and 12-A diodes were operated up to 2.4 MHz and 1 kW, as shown in Figure 5.23b. The 12-A diode notably increased the efficiency at heavy loads, resulting

![Diagram](image)

**Figure 5.23** – The trade-off between diode current rating and its junction capacitance affects the efficiency of the boost converter based on impulse rectification. (a) $C_J$ versus rated current for SiC Schottky diodes from a same family. (b) $\eta$ versus $P_{IN}$ and $f_{SW}$ for converters designed with 4-A, 8-A and 12-A rated diodes. At light loads, the reactive power of $C_J$ limits the efficiency, whereas at heavy loads, conduction loss becomes dominant.
in a peak efficiency of 98.6%. This is because at high power, \( f_{SW} \) is relatively low and conduction loss is dominant. Therefore, utilizing diodes with higher rated currents improves the efficiency. At light loads (\( f_{SW} > 2 \text{ MHz} \)), the diode with lower \( C_J \) (i.e. the 4-A device) generates less reactive power, enabling a higher \( \eta \). For all the cases, the toroidal air-core inductor with S675/AWG48 Litz wires was employed.

### 5.2.6 Control Strategy for Maximizing the Efficiency

Losing ZVS at high frequencies can result in transistor failure due to excessive thermal and electrical stresses. In impulse rectification regime, we discussed that the power of the boost converter is regulated by frequency; therefore, applying an optimum duty cycle \( D_{OPT} \) at each frequency is essential to the safe and efficient operation of the converter.

![Graph](image)

**Figure 5.24** – Optimum duty cycle pattern for control of the boost converter based on impulse rectification mode. (a) \( D_{OPT} \) is a logarithmic function of \( P_{IN} \) for a fixed voltage gain. (b), (c) coefficients \( A(G) \) and \( B(G) \) versus \( G \), used to determine \( D_{OPT} \) for a given voltage gain based on (5.18). Optimum duty cycle control is essential to maintain ZVS for a safe and efficient operation of the boost converter in impulse rectification mode.
For $D$ values greater than $D_{OPT}$, soft switching is compromised. For $D < D_{OPT}$, less charging time is provided to the inductor which results in a lower power transfer and consequently reduced efficiencies, especially under light-load high-gain operations [55].

Figure 5.24a presents the $D_{OPT}$ for the designed boost converter at various $G$ values and different power levels. $D_{OPT}$ can be extracted as function of input power and voltage gain as

$$D_{OPT}(P_{IN}, G) = A(G)\ln(P_{IN}) + B(G)$$  \hspace{1cm} (5.18)

At a fixed gain, $D_{OPT}$ is a logarithmic function of $P_{IN}$. One can formulated coefficients $A(G)$ and $B(G)$ in (5.18) as

$$A(G) = c_0 + \frac{c_1}{1 + (\frac{G}{c_2})^{c_3}}$$  \hspace{1cm} (5.19)

$$B(G) = d_0 + \frac{d_1}{1 + (\frac{G}{d_2})^{d_3}}$$  \hspace{1cm} (5.20)

in which $c_0$ to $c_3$ and $d_0$ to $d_3$ are constants extracted from the fitting of (5.19) and (5.20) to the experimental data, as shown in Figures 5.24b, 5.24c. By utilizing (5.18) in a real-time controller or deriving a look-up table and hard coding $D_{OPT}$ values, the efficiency of boost converters in impulse rectification mode can be maximized, which in turn eliminates the risk of device failure due to hard switching and thermal runaway.

### 5.2.7 System-Level and Transistor-Level Loss Breakdown

The efficiency of the boost converter with the S675/AWG48 air-core inductor and the 12-A diode reached a maximum of 98.6% (corresponding to $G = 2.3$ and $P_{IN} = 431.2$ W). Also, $\eta > 98\%$ was maintained up to $P_{IN} > 1$ kW (see Figure 5.23b).

To identify the efficiency bottleneck, a comprehensive loss breakdown was performed using the inductor HF resistance measurement, spice models for the transistor and diode and their combination with the measured soft-switching losses of the GaN transistor based on the conditions presented in Chapter 2 [27].

The inductor was modeled by its parameters extracted from the small-signal $Q$ measurements (see Figure 5.21). Figure 5.25a presents a system-level loss breakdown at the most efficient operating point of the converter. At $f_{SW} = 1.6$ MHz and a peak current of 6 A, the inductor contributes to more than half of the overall converter losses. Despite its relatively high $Q$ ($Q > 200$, see Figure 5.22b), the inductor is still the bottleneck for obtaining higher efficiencies (and of course higher power densities). Development of new magnetic materials with better HF properties (as mentioned in Chapter 3) is key to higher efficiencies and
Chapter 5. Enhanced Soft-Switching DC-DC Topologies

Figure 5.25 – System-level and transistor-level loss break down for the boost converter based on impulse rectification at its most efficient operation. (a) System loss breakdown at $f_{SW} = 1.6$ MHz and $P_{IN} = 431.2$ W with $\eta = 98.6\%$. The inductor is the efficiency bottleneck. (b) Transistor loss breakdown for GS66508B according to the measurement results from Chapter 2 [27].

power densities in converters based on inductive power transfer.

By applying the measurement results introduced in Chapter 2, we derived an approximation of the losses originated from the transistor conduction and dynamic $R_{DS(ON)}$ degradation, as well as gate and output capacitance losses [27, 64, 75]. Figure 5.25b illustrates the loss breakdown. Based on this approximation, device conduction losses amount to more than 60% of the overall losses. The two other major sources of power dissipation include the effect of dynamic $R_{DS(ON)}$ degradation and $C_{OSS}$ loss.

Although ZVS in the boost converter presented in this chapter satisfies the assumptions of soft-switching loss evaluations in Chapter 2, there are some differences worth further investigation to accurately determine the share of each transistor loss component. For example, $C_{OSS}$ loss in Figure 5.25b has been extracted based on the simplifying assumption that $V_{DS}$ is a single-tone sine waveform at a frequency equal to the converter switching frequency (i.e. $f_{SW} = 1.6$ MHz). $R_{DS(ON)}$ and its degraded value are extracted from the tests performed on the GS66508T transistor in Chapter 2 at a test current similar to that of the boost converter in its most efficient operation, but with different timings.

Interestingly, electrical parameters from datasheets of GS66508T (top cooled) and GS66508B (bottom cooled) GaN devices are similar but they seem to have different $C_{OSS}$ losses [73]. This becomes relevant since for the studies in Chapter 2, the GS66508T device was tested, whereas for the high-density boost converter design in this chapter, the bottom-cooled GS66508B device was employed for its better heat transfer to the IMS PCB.

5.2.8 Benchmarking the Converter Efficiency and Power Density against the State-of-the-Art

In Figure 5.26, the boost converter based on impulse rectification is benchmarked against state-of-the-art DC-DC converters in terms of peak efficiency and volumetric power density [52, 61, 95, 133, 141–157].

The red stars indicate three generations of HF DC-DC converters developed as a part of this research.
5.2. Optimized Boost Converter Based on Impulse Rectification

Figure 5.26 – Benchmarking DC-DC converters (with power levels of up to several tens of kilowatts) in terms of peak efficiency and volumetric power density [52, 61, 95, 133, 141–157]. The red stars correspond to the DC-DC converters developed as a part of this thesis (i.e. PSFB, E-DAB and boost based on impulse rectification). By applying the bottom-up design improvements presented over the course of the thesis, efficiency and power density were continually increased, with the optimized boost converter in impulse rectification mode outperforming state-of-the-art.

work, whose efficiency and power density were continually increased thanks to the use of WBG devices and applying the bottom-up design improvement guidelines in the previous chapters. The first generation corresponds to a PSFB isolated converter with a peak efficiency of 94% and a peak power density of 30 W/inch\(^3\), which was briefly discussed in Chapter 3. The second generation was the E-DAB converter presented at the beginning of this chapter, whose peak efficiency and power density reached 97.4% and 164 W/inch\(^3\), respectively. Last, but not least, the boost converter based on impulse rectification outperformed the state-of-the-art with an ultrahigh efficiency and power density of 98.6% and 850 W/inch\(^3\), respectively.

5.2.9 Conclusion

The operation of boost converters based on impulse rectification and the governing equations for this regime were introduced. Impulse rectification mode offers soft-switching for the transistor (unlike in CCM) and the power transfer is regulated with frequency (unlike in DCM).

To demonstrate the full potential of the topology, a MHz-class kilowatt-range boost converter based on impulse rectification was optimized for high efficiency and high power density, using high-performance GaN transistors and SiC Schottky diodes with zero reverse recoveries. A compact single-layer PCB design based on IMS technology enabled a superior thermal conductivity of \(k_t > 60 \text{ W/m·K}\).

A comparison between different geometries and HF materials resulted in designing wide-BW toroidal air-core inductors. It was shown that higher number of Litz wire strands in the air-core inductors increases the peak of quality factor and reduces the bandwidth, which can be adjusted to maximize the efficiency at
different power levels.

Using diodes with higher current ratings resulted in better efficiencies at high power levels; nonetheless, the major trade-off was the increased reactive power which degraded light-load efficiencies.

We introduced an optimum duty cycle control strategy which maximizes the efficiency at any given operating point and prevents the risk of transistor failure due to an unwanted hard switching at extremely high frequencies.

A detailed loss breakdown in system level identified the inductor losses as the efficiency bottleneck, and based on the results from Chapter 2, transistor-level loss components were estimated. Such a loss breakdown is of great significance to the improvement of WBG semiconductor devices as well as power converters based on WBG technologies.

The boost converter was benchmarked against state-of-the-art DC-DC converters, exhibiting an excellent figure of merit with a peak efficiency of 98.6% at an ultrahigh power density of 52 kW/l (850 W/inch$^3$).
6 Conclusion and Future Directions

6.1 Conclusion

Achieving high efficiencies and large power densities for power converters have been made possible with the emergence of high-performance WBG technologies. Nonetheless, realizing the full potential of these technologies requires fundamental analyses and optimizations in several levels of design. Figure 6.1 summarizes the bottom-up approach followed in this thesis - to maximize the efficiency and power density in high-frequency converters and pulsed-power generators at different levels of design - as:

The base level is the proper characterization of power transistors, which was the subject of Chapter 2. The main challenge is that datasheets from commercial WBG device manufacturers neglect some of the most important performance parameters for HF, VHF and pulsed operations of power transistors. Among them are the gate losses for soft-switching transistors, dynamic ON-resistance degradation and output-capacitance losses. In Chapter 2, the existing knowledge from the literature is combined with new measurement methods to evaluation switching speeds and soft-switching losses in GaN and SiC FETs. The analyses, tools and methods presented in Chapter 2 enable a designer to choose a WBG transistor based on the specifications of target applications. It also enables device engineers to properly characterize and constantly improve WBG devices.

Another fundamental aspect, which is as important as, if not more, than proper transistor characterization, is the design of magnetic components at high frequencies. Many power converter topologies are based on inductive power transfer, and the selection of proper magnetic materials and geometries are crucial to their compact design and efficient operation of inductors and transformers. First in Chapter 3, we discussed about major sources of losses in HF magnetic components and provide a comparison between ferrites. Next, the pros and cons of simulation methods (i.e. FEA) and small-signal quality factor measurements were reviewed with specific case studies. Finally, we concluded that although such methods are useful design tools, they lack accuracy for evaluation of low losses in magnetic components under large-signal HF circuit operations, highlighting the need for more precise and general measurement techniques.

To bridge the gap between the need for accurate loss measurement methods and limitations of existing techniques, in Chapter 4 a novel calorimeter with an unprecedented accuracy and measurement range was introduced. The special design of the calorimeter enabled calibration-free measurement of low losses in HF components (such as losses in high-quality inductors), as well as efficiencies in high-performance
Chapter 6. Conclusion and Future Directions

Figure 6.1 – The bottom-up approach suggested in the thesis to maximize the efficiency and power density of HF power electronics systems. Chapter 2 deals with the characterization and comparison of switching speed and soft-switching losses in WBG devices. Chapter 3 is dedicated to the evaluation of high-quality magnetics at HF. In Chapter 4, novel calorimetric techniques are used to accurately measure low losses and high efficiencies. Chapter 5 introduces topology improvements.

power electronics systems (such as DC-DC converters). A second approach based on temperature mapping was utilized to quantify the losses and their distribution over different circuit components. Experimental case studies verified the usefulness of the methods for measurement of HF inductor losses, as well as the evaluation of gate losses for soft-switching GaN transistors at VHF operation.

After characterizing the most important parameters of WBG devices and providing accurate measurement tools for capturing the losses in magnetic components and circuits in Chapters 2 to 4, high-level topology enhancements were proposed. First, by equipping a DAB topology with tapped HF transformers, an enhanced DAB (or E-DAB) converter was realized, which extended soft-switching and voltage gain ranges significantly, without introducing any extra losses to the system, or adding modulation complexities. Next, a new operation mode for boost converters was introduced to significantly extend the efficiency and power density compared to the traditional CCM or DCM operation modes. Converters based on both topologies were benchmarked against state-of-the-art power converters, showing outstanding figures of merit with 97.4% peak efficiency and 10 kW/l for the E-DAB converter, and 98.6% peak efficiency and 52 kW/l for the boost converter.

As a summary, the thesis provides a strong connection between power semiconductors and their characteristics (bottom-level design), magnetic components and their loss evaluation methods, and enhanced topologies and their control (high-level design), with the main focus on increasing the overall efficiency and power density. The measurement methods shed light on proper WBG technology and magnetic component characterization, and provide insights for improving the performance in new generations of those components. The presented topologies and control concepts open new horizons for future ultra-efficient and high-density power conversion systems.
6.2 Future Directions

The main objective of this thesis was to discover the limits of efficiency and power density for power converters based on WBG technologies. Furthermore, the obtained results are extremely useful to the improvement of WBG devices and magnetics materials for future HF power converters. Based on the presented work and the main objective of this thesis, the following directions are suggested for further research:

- Time-domain simulation tools such as SPICE are incredibly useful for assessing the general performance of a system; nonetheless, models for WBG transistors are incomplete in several ways. For instance, they neglect the effects such as dynamic ON-resistance degradation or output-capacitance losses. The measurement tools and results presented in Chapter 2 are extremely useful for developing comprehensive device models. Also device engineers can focus their research topics on the improvement of new generations of WBG transistors for low-loss HF and VHF operations.

- Based on the results presented in Chapters 3 and 5, air-core inductors (similarly transformers with sufficient leakage inductances) offer higher BW and $Q$ factors for HF applications. An automated algorithm can be developed to tune the inductor and transformer designs for achieving any target $Q$ factor and BW. Modeling of capacitive effects of ferrite cores and windings in magnetic components is another interesting topic, which is at the same time of great significance to HF and VHF applications. In other words, research on developing a generalized model which takes into account both the losses and the parasitic elements of power magnetics is a worthwhile future direction.

- By using the calorimeter presented in Chapter 4, losses down to 500 mW could be measured. By scaling down the proposed calorimeter and using more accurate temperature sensors, one can achieve exceptionally high accuracies in measurement of power losses. Furthermore, investigating methods to reduce the measurement times based on the proposed concept would be highly valuable, especially for industrial applications.

- A loss measurement method based on temperature mapping was presented in Chapter 4. A promising future direction would be to develop an automated image processing tool, which can be trained based on a few calibration tests, and can extract the losses for every single component in a given circuits at different operating conditions, regardless of the count of the components.

- With the growing demand for higher power densities, and as a result of increased switching frequencies, developing application-specific integrated circuits or digital processors with integrated high-bandwidth measurement tools (similar to probes) could be a promising direction.
The PCB schematic for voltage rise rate measurements of the GS66508T GaN transistor in Chapter 2, Figure 2.3a will be presented here.

Figures A.1, A.2 show the gate driver circuitry and the half bridge power stage, respectively. The PWM signals are issued using the TMS320F28379D DSP board which was previously presented in Figure 4.13a. For measuring the VRR of other transistors (i.e. SiC, Si and Si-SJ), a similar gate driver was used. Apart from the GaN device which came in a surface mount package, the leads of other transistors (with TO-247 packages) were cut as short as possible to minimize the gate-drive and power loop inductances.

For the CRR measurements, we utilized the PCB presented in Chapter 2, Figure 2.8b. The detailed schematic of this circuit comes in Figure A.3. PWM signal is isolated from the power stage by using SI8271 isolated gate drivers. Two isolated DC source provided the supply voltage to the gate driver. Circuit ground was connected to the external supplies such that the transistor could be turn-OFF with a negative voltage. Sixty thick-film pulsed resistors were placed in parallel to form a low-inductance 6-Ω resistive load. 6-Ω was chosen as the load so that the test currents can get close to the saturation limit of the transistors at 400 V of DC link voltage. A limiting resistor was placed in series with the DC link to protect the DC power source from over currents in the case of a transistor failure (short circuit). A similar PCB was used to evaluate CRR for the SiC transistor investigated in Chapter 2.
Figure A.1 – Schematic of gate driver stage for VRR measurements of Chapter 2. For accurate measurements, gate-drive loop has been minimized in the corresponding layout design.
Figure A.2 – Schematic of the half bridge used to measure VRR for the GS66508T GaN transistor. For accurate measurements, power loop has been minimized in the corresponding layout design.
Figure A.3 – Circuit schematic for the measurements of CRR, including the gate driver circuitry, a GS66508T GaN transistor and the low-inductance 6-Ω resistive load.
System design for the dual-chamber calibration-free calorimeter was described thoroughly in Chapter 4 under Section 4.1. The electrical schematics related to the peripheral management board are presented here, including signal mapping for data acquisition/control and their corresponding LabVIEW codes.

The inputs and outputs to and from the myRIO-1900 FPGA unit are connected to the controller board as shown in Figure 4.4b. Figure B.1 shows the signal allocation for the three buses on myRIO-1900 called MXPA, MXPB and MSPC. The signals are generally assigned to run communication protocols, feedbacks from sensors, commands to the actuators and the human user interface.

In Figure B.2, the control and feedback signals to and from the µ-diaphragm NFB5KTDCB-4 water pump are presented. For immunity to EMI, separate analogue and digital ground planes were placed in the peripheral management PCB. The water flow rate was directly controlled using a LabVIEW human user interface which will be presented later in this section.

Pt.100 is a platinum-based resistance temperature detector technology with a fixed resistance of 100 Ω at 0 °C. Water temperature sensors provide a current which is variable with temperature. In our case, the resulting currents from the water temperature sensors were then converted to voltage signals with amplitudes between 0 V to 10 V (for temperatures between 0 °C to 60 °C) using JUMO dTRANS T03 BU 0C-60C (703030) transmitters. After applying low-pass filters to eliminate HF noises, as shown in Figure B.3, the signals were read by the myRIO-1900. Two signals were measured directly (single-ended respective to the electrical ground), to acquire the absolute temperature values. Two other temperature signals were measured deferentially by the myRIO-1900, enabling a direct extraction of the temperature differences over each of the chambers.

Figure B.4 shows the RS-232 to universal asynchronous receiver-transmitter (UART) interface used for the communication between Fluke 45 dual display DMM (responsible for DC power measurement of the calibrators) and the myRIO-1900. It is worth mentioning that for voltage and current measurements, the calibrator networks must be connected to the voltmeter first, and then the ammeter comes between the DC adjustable source and the calibrator. If otherwise configured, there would be a relatively large voltage drop over the ammeter, which makes the measurements inaccurate (because the voltmeter then measures the sum of actual CAL voltage plus the voltage drop over the ammeter).

The power dissipated in inner fans (inside of each chamber) is measured using INA219BIDR power...
### Appendix B. Calorimeter Electrical Design for the Peripheral Management Board

**Figure B.1 – Signal allocation for three buses on myRIO-1900 FPGA control unit.** The signals are generally assigned to run communication protocols, feedbacks from sensors, commands to the actuators and the human user interface.

Monitoring device using inter-integrated circuit (I2C) communication protocol. A current sensing shunt resistor with a tolerance of ±0.1% and a temperature coefficient of ±15 ppm/°C was used for accurate power measurements. Figure B.5 shows the electrical schematics for the power measurement unit of one of the inner fans, as well as the configuration settings for INA219BIDR.

Figure B.6 shows the auxiliary power jack for a 5-V DC input, and its conversion to 3.3 V, which were used to deliver power to different units such as controllers, communication units and measurement devices.

A LCD display was as a part of the human user interface. Serial peripheral interface (SPI) protocol was...
Figure B.2 – Control and feedback signals to and from the μ-diaphragm NFB5KTDDB-4 water pump. The detailed electrical and mechanical operating conditions of the pump can be found in the manufacturer user manual. For immunity to the EMI, separate analogue and digital ground planes are utilized in the controller PCB. The water flow rate can be directly controlled using a LabVIEW human user interface.

used for communication between the myRIO-1900 and the LCD, as shown in Figure B.7. The LCD can be programmed to display the measurement time, water temperature gradients and the measured power loss detected in the DUT chamber in a real-time manner.

Figure B.3 – Single-ended signals from Pt.100 water temperature sensors and the applied low-pass filters. The low-pass filters were used to eliminate HF noises.
Figure B.4 – RS-232 to UART interface used for data transfer between Fluke 45 as the CAL power measurement unit and myRIO-1900.
Figure B.5 – Schematic for the power monitoring unit of inner fans using INA219BIDR. I2C protocol was used for communication. A shunt resistor with a very low tolerance (±0.1%) and extremely small temperature coefficient (±15 ppm/°C) was selected for accurate power measurements.

Figure B.6 – Through an auxiliary power jack, a 5-V DC input was provided and then converted to 3.3 V. This was to deliver power to different units such as controllers, communication units and measurement devices.
Figure B.7 – Schematic for SPI communication with the LCD used as a part of the human user interface. The LCD can be programmed to display the measurement time, water temperature gradients and the measured power loss detected in the DUT chamber in a real-time manner.
Figure B.8 – Front panel design in LabVIEW environment for control and monitoring of the calorimeter.
Figure B.9 – Block diagram window for the user interface developed in LabVIEW for automating the measurements. The automation includes data acquisition for temperatures, the PI regulator, the calibrator power detector and the set point provider for driving the adjustable DC source.
Figure B.10 – LabVIEW block diagram for the calibrator power reading with Fluke 45 DMM and sending commands to the adjustable DC source and water pump. (a) Settings for the block diagrams used to communicate with the Fluke 45 DMM. CAL current and voltage are measured and the power of the CAL is extracted based on the two consecutive DC measurements. (b) Settings for sending the control commands to the adjustable DC source (for power tracking) and the water pump (for flow rate adjustment).

The system was fully automated, and all the parameters were configurable/able to be monitored via the user interface developed in LabVIEW environment, as shown in Figure B.8. The block diagram presented in Figure B.9 includes the interconnection of different code building blocks such as data acquisition for the temperatures, the PI regulator, the calibrator power detector and the set point provider for driving the adjustable DC source. The calibrator power measurement was performed using the Fluke 45 dual display DMM. The block diagram for communicating with Fluke 45 is presented in Figure B.10a. The command signals were sent to the controllable DC source and the water pump based on the diagram shown in Figure B.10b.
C PCB Schematics for the DC-DC Power Converters

In this section, schematics for the power converters of Chapter 5 are presented.

Figure C.1 shows the driving stage of the E-DAB converter for one of the high-side transistors in the primary full bridge. A fully isolated design was realized using SI8271 gate drivers and ADUM5000 isolated auxiliary DC-DC converters. The same architecture was employed for driving all the eight switches in the primary and secondary full bridges. The signal and power sides were galvanically isolated, enabling a robust control and safe operation of the converter.

Figure C.1 – Schematic of the driving stage for a high-side transistor in the E-DAB converter. The same architecture was employed for driving all the eight switches in the primary and secondary full bridges. The signal and power sides were galvanically isolated, enabling a robust control and safe operation of the converter.
switches in the primary and secondary full bridges. For a robust and independent operation of transistors in each leg, we decided not to use bootstrap configuration; still a compact design was realized. The corresponding four-layer PCB layout which was discussed in Chapter 5, enabled the minimization of gate and power-loop inductances.

In Figure C.2, the schematic for gate driver and power stages of the ultra-dense boost converter based on impulse rectification is presented. The power and gate-drive stages in this design are non-isolated. To achieve a compact design on a single-layer IMS PCB, we used the UCC27611 gate driver for driving the GS66508B GaN transistor. As it was discussed in Chapter 5, a comprehensive analysis was performed to optimize the inductor and its BW to maximize the conversion efficiency. The aluminum PCB substrate was electrically connected to GND to eliminate any stray capacitances which could disturb the circuit performance.
Bibliography


Bibliography


Bibliography


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RESEARCH INTERESTS


RESEARCH INTERNSHIP

Research Intern
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Lausanne, Switzerland
Supervisor: Prof. Elison Matioli
January-June 2017

• Design and finite-element (COMSOL) simulation of HF planar transformers
• Realization of a 400-W PSFB soft-switched micro converter based on GaN transistors and SiC Schottky diodes. Using this optimized DC-DC converter, a compact size, high efficiency, and robust control was achieved, highly instrumental to the integration of consumer electronics with PV energy resources in the future DC microgrids at distribution level
PROFESSIONAL EXPERIENCE

Electrical Designer 2017-2018
EPFLOOP (EPFL Hyperloop Team) Lausanne, Switzerland

• Coordination and execution of electrical and in part mechanical design for subcomponents (motor, drive, UPS, controller, various sensors, and actuators), with military-grade safety and resilience
• Partnership with industry for sizing and verification of batteries and BMS for the hyperloop EV

Software Automation Engineer 2016-2017
Behpoo (Industrial Machinery) Tehran, Iran

• Development of a user interface for control and calibration of industrial feeders
• Hardware design for position/speed control of servo motors used in ready-to-market products

TEACHING EXPERIENCE

Energy Conversion 2017-2020
EPFL

Physics II (Electromagnetics) 2013-2016
Microprocessors
Signals and Systems
Electrical Machines I/II
Electrical Circuits II
Power Systems Analysis I
Industrial Electronics
University of Tehran

LANGUAGES

Persian  Mother tongue
English  C1
German  B2
French  B1/B2
HONORS & AWARDS

**ECCE Asia Best Paper Award**
In recognition of the paper entitled as:
*Enhanced DAB Converter: Comprehensive Design Evaluation*

2020

**Winner of SpaceX Hyperloop Competition**
EPFLop (EPFL hyperloop team) achieved 3rd-place for speed and 1st-place for safety.
I contributed to the electrical design and energy delivery, among other tasks.
*EPFL, Lausanne, Switzerland*

2018

**Best Teaching Assistant Award**
Given course: Power Systems Analysis I
*School of Electrical and Computer Engineering, University of Tehran, Iran*

2016

**Professor Mohseni’s Award**
In recognition of: Phasor measurement unit for overload protection of power transformers
*High-Voltage Laboratory, School of Electrical and Computer Engineering, University of Tehran, Iran*

2015

**IEEE Best Project Award**
For the development of: Ultrasonic Distance-Meter (Microprocessor-Based Design)
*IEEE Student Branch, University of Tehran, Iran*

2014

REVIEWS

*IEEE Transactions on Power Electronics*

*IEEE Sensors Journal*

*IEEE Transactions on Industrial Informatics*