Performance Analysis of a Hybrid Incremental and Cyclic A/D Conversion Principle

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***Abstract*—This paper presents a new hybrid A/D conversion principle based on the combination of an incremental conversion for the most significant part of the result and on a cyclic conversion for the least significant part. The proposed approach exhibits a resolution comparable to a multiorder sigma–delta A/D converter (ADC), but with a higher conversion rate (typically a factor of two) and/or a lower complexity, at the cost of a more stringent antialiasing filter requirement. After having presented the basic equations of the conversion principle, a theoretical analysis of the resolution limitations is given, based on nonidealities and noise considerations. Finally, a switched-capacitor implementation example is given with the corresponding simulations, consisting of a low-complexity 14-b ADC suited for applications requiring medium-speed and very compact ADC.**

***Index Terms*—A/D conversion, cyclic, incremental.**

I. Introduction

CYCLIC OR algorithmic A/D conversion is well known for its ability to achieve medium resolution while requiring a small silicon area and featuring a reasonable conversion speed of one conversion cycle per bit of resolution. It has traditionally been used for general-purpose A/D converters (ADCs), such as microcontroller peripherals or voice applications [1]. Without any calibration or trimming, the resolution of cyclic ADCs is generally limited to 10 b due to nonidealities such as device mismatch or finite operational-transconductance-amplifier (OTA) gain. Well-known techniques have been used to improve the resolution of the cyclic ADC. Ratio-independent (for instance, capacitor averaging) and gain-insensitive algorithms have been proposed [2]–[6], allowing up to 12–14 b of resolution, at the expense of multiple conversion cycles per bit and/or additional active elements. Digital calibration is also being used, allowing up to 15 b of resolution in cyclic [7]–[9] or pipelined ADCs [10], [11], but the important required digital circuit compromises the small silicon area. In all cases, the resolution of the cyclic ADC has shown to be limited to about 15 b.

For higher resolutions, oversampled ADCs are used, allowing up to 20 b [12]. These converters are generally realized by the combination of a sigma–delta modulator [13] and a digital low-pass filter [14]. An alternative oversampling structure is the so-called incremental converter [15], [16]. Although inspired by the dual-slope principle, the analog and digital parts of this ADC present many similarities with the modulator, respectively, the low-pass filter of a sigma–delta converter [17]. One disadvantage of this ADC is that it generally requires a sample-and-hold stage clocked at a much slower speed and, therefore, does not have the relaxed antialiasing filter requirement that conventional sigma–delta ADCs have. It is, however, less prone to jitter noise [18].

Both converters feature an increase in resolution of 1 b for each doubling of the sampling frequency, which makes their resolution increase *logarithmically* with the conversion time. Therefore, they are inherently much slower than the cyclic ADC, for which the resolution increases *linearly* with the conversion time. The speed of these ADCs can be increased by cascading several modulators or integrators [13], [19]. However, for orders higher than two, they generally present stability problems; for the same operating frequency, their conversion rate remains much lower than the cyclic ADC.

In order to fully exploit the distinctive advantages of different conversion principles, cascaded converters have been introduced. Oversampled conversion has been used in the front end for the high-resolution conversion, and the residue has been fed to a pipeline [20], [21] or to a flash converter [22], with a smaller accuracy but a much faster conversion speed.

This paper proposes a new cascaded (or hybrid) converter topology made of an oversampled converter and a cyclic converter. The oversampled stage extracts the most significant bits (MSBs) of the result and produces an analog residual voltage. This voltage is then passed to a cyclic converter, which extracts the least significant bits (LSBs) of the result. This paper shows that this hybrid approach exhibits a resolution comparable with a multiorder sigma–delta ADC, but with a higher conversion rate and/or a lower complexity. For instance, for a 16-b resolution, the proposed second-order structure is two times faster than a second-order sigma–delta ADC. Another advantage of this new topology is that both converters can be realized using the same hardware, thus leading to a very compact converter.

This paper is structured as follows. The proposed ADC principle is fully described in Section II, and a theoretical analysis of its performance is given in Section III. Section IV shows an implementation example featuring a low hardware complexity. The expected performance, based on simulations, is also provided. Finally, Section V presents an overview of the possible applications of this new conversion principle and concludes this paper.

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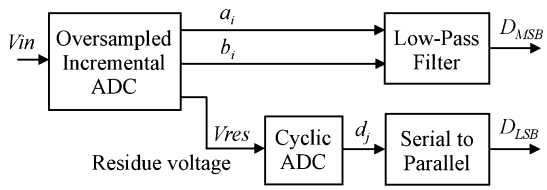

Fig. 1. Proposed conversion scheme.

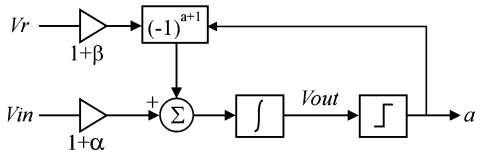

Fig. 2. First-order incremental ADC.

II. Proposed Conversion Principle

The proposed conversion principle, shown in Fig. 1, consists of a two-step conversion scheme. An oversampled incremental ADC [19] is used in the first step, producing one or several digital bitstreams, one for each modulator (the figure shows a two-stage modulator with bitstreams a_i and b_i), which are filtered through a low-pass filter to obtain D_{MSB}, the most significant part of the conversion result. The residue voltage V_{res} of the incremental ADC is fed into a cyclic ADC, producing a serial bitstream d_j, which is transformed into parallel format to obtain D_{LSB}, the least significant part of the result. Because of its integrating properties, the oversampled stage features a low sensitivity to noise and component mismatch and is therefore suited for the MSBs of a conversion. However, such a high resolution is not required for the extraction of the LSBs. Since the same conversion principle is usually applied for all bits, the conversion time of an oversampled ADC is unnecessarily long. The main idea of this paper consists of changing the conversion principle once the MSBs have been extracted and adopting a cyclic conversion scheme, which is much faster, for the remaining LSBs.

A. First-Order Incremental ADC

The incremental ADC used in the first stage is fully described in [19] and consists of sigma–delta modulators which are reset before each conversion. A first-order incremental ADC is shown in Fig. 2, with gain errors α and β on the input voltage Vin and the reference voltage Vr, respectively.

The architecture is based on an integrator and a comparator. Before each conversion, the integrator is reset. Then, for a k-bit resolution, 2^k integration steps are performed. For each step, the input voltage Vin is integrated, and depending on the sign of the digitized integrator output bit a, a reference voltage Vr is added or subtracted to the integrator. At the end of the 2^k steps, the output voltage $Vout$ of the integrator, called the residue voltage, is as follows:

$$Vout_{[2^k]} = (1+\alpha)\cdot 2^k \cdot Vin - (1+\beta)\cdot N \cdot Vr. \quad (1)$$

N corresponds to the number of subtraction minus the number of addition of the reference voltage Vr. Therefore, it is directly the digital representation of the input signal. Practically, the low-pass filter of output bitstream a is implemented by a simple up–down counter, giving number N as result. As explained in [15], any systematic offset error at each integration step can be compensated using a double integration scheme of 2^{k-1} integration steps each (the second one using an inverted input voltage), separated by the inversion of the residue voltage, giving the residue voltage

$$Vout_{[2^k]} = -(1+\alpha)\cdot 2^k \cdot Vin + (1+\beta)\cdot (N_{\mathrm{pos}} - N_{\mathrm{neg}})\cdot Vr \quad (2)$$

where N_{pos} and N_{neg} are the up–down counts of the first and second integration periods, respectively. It is worth noting that the amplitude of this residue corresponds to the input range of the ADC ($-Vr$ to $+Vr$); thus, an amplification is not required if the residue is to be passed to a subsequent stage, as proposed.

The number of cycles P_{inc1} needed for k bits of resolution is as follows:

$$P_{\mathrm{inc1}} = 2^k + 1. \quad (3)$$

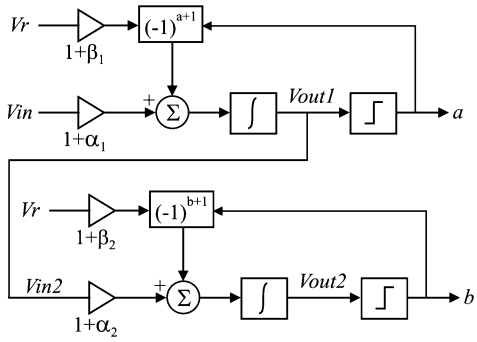

Fig. 3. Second-order incremental ADC.

B. Second-Order Incremental ADC

The incremental ADC previously described can be easily cascaded with a similar stage [19], to obtain a second-order incremental ADC (Fig. 3), equivalent in its principle to a second-order multistage sigma–delta modulator and resulting in a considerable reduction of the conversion time.

A conversion begins with a reset operation of the two integrators, followed by an integration step of the first stage, giving the residue voltage $Vout$. Then, p integration steps are performed, during which, both first and second stages integrate their input signals, i.e., Vin for the first stage and $Vout$ for the second stage. At the end of the p cycles, one more integration step is needed for the second stage to complete p cycles. Then, similarly to the first-order case, the output voltage of the first integrator is reset, while the residue $Vout2$ of the second stage is inverted. Another $p+1$ integration steps are performed with an inverted input voltage Vin. The total number of cycles P_{inc2} required for k bits of resolution is as follows:

$$P_{\mathrm{inc2}} = 2p + 2 = 2^{k/2} + 2. \quad (4)$$

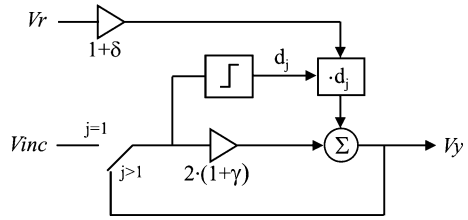

Fig. 4. Cyclic ADC principle.

Assuming gain errors of α_2 and β_2 on the input and reference voltages of the second stage, respectively, the residue voltage $Vout2$ of the integrator, after $p+1$ steps, is as follows:

$$\begin{aligned} Vout2_{[p+1]} = &\frac{p\cdot(p+1)}{2}(1+\alpha_1)\cdot(1+\alpha_2)\cdot Vin \\ &-(1+\beta_1)\cdot(1+\alpha_2)\cdot\sum_{i=1}^{p}a_i(p+1-i)\cdot Vr \\ &-(1+\beta_2)\cdot\sum_{i=2}^{p+1}b_i\cdot Vr. \end{aligned} \tag{5}$$

The residue voltage $Vout2$ is inverted, and $p+1$ integration steps are performed, this time with an inverted input voltage. After $2p+2$ integration steps, the residue voltage $Vout2$ is as follows:

$$\begin{aligned} &Vout2_{[2p+2]} \\ &\quad= p(p+1)\cdot(1+\alpha_1)\cdot(1+\alpha_2)\cdot Vin \\ &\qquad-(1+\beta_1)\cdot(1+\alpha_2)\cdot\sum_{i=1}^{p}a_i(p+1-i)\cdot Vr \\ &\qquad-(1+\beta_1)\cdot(1+\alpha_2)\cdot\sum_{i=p+2}^{2p+1}a_i(p+1-i)\cdot Vr \\ &\qquad-(1+\beta_2)\cdot\sum_{i=2}^{p+1}b_i\cdot Vr-(1+\beta_2)\cdot\sum_{i=p+3}^{2p+2}b_i\cdot Vr. \end{aligned} \tag{6}$$

C. Cyclic ADC

The cyclic ADC conversion principle is usually implemented as in Fig. 4, where j conversion cycles are performed. During the first cycle ($j=1$), the input voltage $Vinc$ is evaluated by a comparator to get bit d_1 of the result: $d_1=1$ if $Vinc>0$; otherwise, it is zero. $Vinc$ is multiplied by two, and an addition/subtraction of a reference voltage Vr takes place: If $d_1=1$, Vr is subtracted; otherwise, it is added. The residue Vy is then looped back to the input for extracting the successive bits d_j of the result. The conversion is performed sequentially from the MSB to the least significant one. The number of cycles is proportional to the resolution.

In this paper, we propose the use of the redundant signed digit (RSD) cyclic algorithm [3], offering the advantage to tolerate large comparator offsets, thanks to decision-level overlaps between successive cycle conversions. In this scheme, a double comparator is used, giving a ternary result d_j, which can take the values 1, 0, or -1, and leading to three possible reference voltage operations: If $d_j=1$, Vr is subtracted; if $d_j=-1$, Vr is added; if $d_j=0$, no reference voltage operation is performed. The redundant serial bitstream is converted into a binary representation with additional logic. At each cycle, the residue voltage Vy is affected by the errors γ and δ as in the following equation. After the first cycle, we have

$$Vy_{[1]} = 2\cdot(1+\gamma)\cdot Vinc - d_1\cdot(1+\delta)\cdot Vr. \tag{7}$$

Moreover, for an n-bit conversion, requiring $n-1$ cycles, we have

$$\begin{aligned} Vy_{[n-1]} = &(2\cdot(1+\gamma))^{n-1}\cdot Vinc \\ &-(1+\delta)\cdot\sum_{j=1}^{n-1}d_j\cdot(2\cdot(1+\gamma))^{n-1-j}\cdot Vr. \end{aligned} \tag{8}$$

For an n-bit conversion, the number of cycles required is

$$P_{\text{cycl}} = n-1. \tag{9}$$

Thus, at the end of the conversion, we have

$$\begin{aligned} Vy_{[n-1]} = &(2\cdot(1+\gamma))^{n-1}\cdot Vinc \\ &-(1+\delta)\cdot\sum_{j=1}^{n-1}d_j\cdot(2\cdot(1+\gamma))^{n-1-j}\cdot Vr. \end{aligned} \tag{10}$$

D. Cascading Incremental and Cyclic ADCs

In the proposed conversion scheme in Fig. 1, the n-bit cyclic ADC is used to convert the residue voltage $Vout$ (for the first order) or $Vout2$ (for the second order) of the k-bit incremental ADC, giving an overall resolution $m=k+n$. In a practical implementation, a perfect output to input amplitude matching between the two cascaded converters must be guaranteed to avoid nonlinearity effects. Since the amplitude of the residue voltage of the incremental ADC may go above $+Vr$ or below $-Vr$ (due to comparator offset), an over-range input capability for the cyclic ADC must be provided. This feature can be implemented by inserting a supplementary cycle at the beginning of the cyclic conversion, during which a reference addition/subtraction is performed on a nondoubled input voltage. The nonidealities of this extra cycle will be included in the analysis of Section III. The total number of cycles per conversion as a function of the resolutions k and n is given by

$$P_{\text{tot1}} = 2^k+n+1 \quad \text{(first order)} \tag{11}$$

$$P_{\text{tot2}} = 2^{k/2}+n+2 \quad \text{(second order)}. \tag{12}$$

Assuming ideal ADCs (no mismatch and no thermal noise), the number of cycles per conversion as a function of the theoretical resolution is shown in Fig. 5 for four different configurations of the proposed hybrid converter (first and second orders with 6 or 8 b of cyclic resolution n) and for the pure incremental first- and second-order approaches [19]. For comparison, the curves of sigma–delta first to third orders are also shown. For these, the relations(13)–(15) are used [24] for the number of cycles per conversion as a function of the resolution k. For the

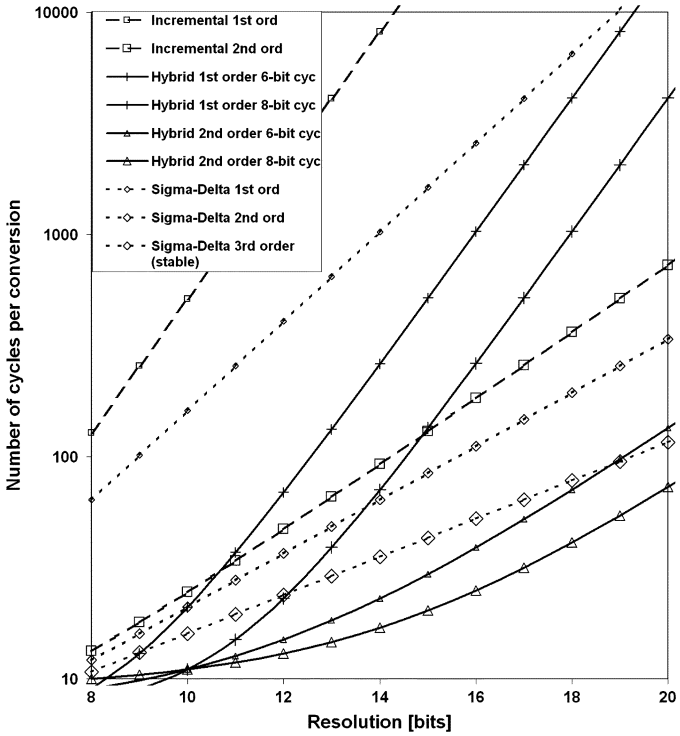

Fig. 5. Theoretical number of cycles per conversion as a function of resolution, for first- and second-order incremental ADCs, a first-order incremental ADC followed by 6- and 8-b cyclic ADCs, and a second-order incremental ADC followed by 6- and 8-b cyclic ADCs. For comparison, sigma–delta ADC curves are also plotted, with first-, second-, and third-order (stable structure corresponding to a typical 1-1-1 MASH ADC) ADCs.

third-order case, stability considerations are taken into account by a decreased resolution of 3 b compared to the ideal quantizer noise-only case [23]. The resulting curve is similar to a 1-1-1 or 2-1 typical MASH sigma–delta ADC structure [25], [26]

$$P_{\mathrm{sd1}} = 2^{\frac{2}{3}(k+1)} \quad \text{(first order)} \tag{13}$$

$$P_{\mathrm{sd2}} = 2^{\frac{2}{5}(k+1)} \quad \text{(second order)} \tag{14}$$

$$P_{\mathrm{sd3}} = 2^{\frac{2}{7}(k+4)} \quad \text{(third order).} \tag{15}$$

In this figure, we see that the proposed first-order structure performs faster, for all resolutions, than the pure incremental or sigma–delta ADC of the same order. The proposed second-order structure is even faster than a stable third-order sigma–delta structure up to a resolution of 18 b.

III. Theoretical Error Analysis

This section analyzes the effect of parameters α, β, α_2, β_2, γ, and δ (gain and reference errors) on the overall resolution of the proposed converter. Like in any subranging ADC, any difference between the output range Ao of the first stage residue and the input range Ai of the second stage causes differential nonlinearity error: $Ao < Ai$ causes missing codes [negative differential nonlinearity (DNL)], while $Ao > Ai$ causes missing decision levels (positive DNL) Fig. 6.

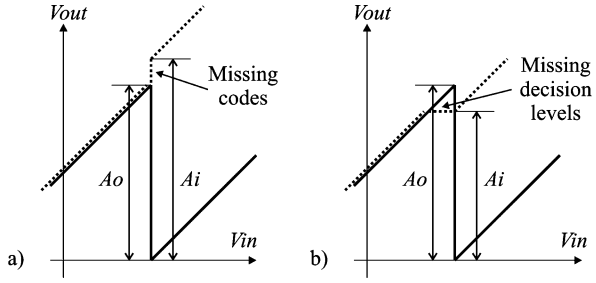

Fig. 6. First-stage output residue $Vout$ as a function of (solid line) its input Vin and (dashed line) corresponding second-stage result in case of an interstage amplitude mismatch: (a) $Ao < Ai$ causes missing output codes, while (b) $Ao > Ai$ causes missing decision levels.

A. Cyclic Conversion

We first consider the cyclic RSD conversion inaccuracies with, in the first step, the influence of parameter γ. The first effect of this doubling error is the generation of a nonlinearity with a maximal value located at the MSB transitions of the cyclic conversion, corresponding to the comparator thresholds (usually $+Vr/4$ and $-Vr/4$), where the same input voltage can give two different ternary codes having the same binary result. The corresponding codes are $[1,-1,0,0,\ldots,0]$ and $[0,1,0,0,\ldots,0]$ (from the MSB to the LSB). With an ideal converter, these codes would give two identical residue voltages Vy' and Vy''. From (7) and after $n-1$ cycles, we have

$$\begin{aligned} Vy' = {} & (2\cdot(1+\gamma))^{n-1}\cdot Vinc - (2\cdot(1+\gamma))^{n-2}\cdot Vr \\ & + (2\cdot(1+\gamma))^{n-3}\cdot Vr \end{aligned} \tag{16}$$

$$Vy'' = (2\cdot(1+\gamma))^{n-1}\cdot Vinc - (2\cdot(1+\gamma))^{n-3}\cdot Vr. \tag{17}$$

The difference between these two values is as follows:

$$Vy''-Vy' = Vr\cdot\left(2\,(2(1+\gamma))^{n-3} - (2(1+\gamma))^{n-2}\right). \tag{18}$$

If we divide this difference by Vr, we obtain the maximal intrinsic nonlinearity error of the cyclic RSD ADC, occurring at the MSB transitions of the cyclic conversion

$$\Delta_{\gamma C1} \cong \gamma\cdot 2^{n-2}. \tag{19}$$

The second effect of parameter γ is the introduction of an overall gain error which affects the amplitude matching between the first and second stages and, hence, the introduction of DNL errors at the first stage residue voltage transitions: If $\gamma > 0$ (amplification), missing decision levels appear; if $\gamma < 0$ (attenuation), missing codes appear. To analyze this error, we take the maximum input signal value, corresponding to an input of $+Vr$. The binary output code is $[1,1,\ldots,1]$, and the obtained voltage is as follows:

$$Vy_{[n-1]} = (2(1+\gamma))^{n-1}\cdot Vr - \sum_{j=1}^{n-1} d_j\cdot(2(1+\gamma))^{n-1-j}\cdot Vr. \tag{20}$$

When $\gamma \neq 0$ and after $n-1$ cycles, this voltage is as follows:

$$Vy_{[n-1]} = Vr \cdot (1 + \gamma \cdot (2^n - 2)). \tag{21}$$

The cumulated gain error is four times bigger than the previous error at the MSB transitions of the cyclic conversion and appears at each first-stage residue voltage transition

$$\Delta_{\gamma C2} = \gamma \cdot (2^n - 2) \cong \gamma \cdot 2^n. \tag{22}$$

The second error parameter δ of the cyclic converter modifies the reference voltage of the cyclic conversion and, therefore, also degrades the interstage voltage matching, producing DNL errors at the first-stage residue voltage transitions. Since it is doubled at each cycle, its value is as follows:

$$\Delta_{\delta C} = -\delta \cdot 2^n. \tag{23}$$

B. Extra Cycle Errors

The amplitude matching between the first (incremental) and second (cyclic) stages of the proposed structure requires an over-range capability for the RSD converter. This can be performed simply by an extra cyclic conversion without the doubling operation, with the following:

$$Vy_{[j]} = (1+\gamma) \cdot Vinc - d_j \cdot (1+\delta) \cdot Vr + Vy_{[j-1]}. \tag{24}$$

The location in time of this extra cycle influences the dynamic of the input range and the obtained gain error. In the normal case, the converter input range is $[-Vr, +Vr]$. If the extra cycle occurs before the first cycle, the dynamic of the converter will be increased by Vr on both sides of its range, leading to an input range of $[-2Vr; +2Vr]$. If it is done before the second cycle, the maximum input signal dynamic will be $+3/2Vr$, etc. The input range of the converter can thus be described with the following, where j represents the location of the extra cycle in the cyclic conversion:

$$\left[\left(-1 - \frac{1}{2^{j-1}}\right) \cdot Vr; \left(1 + \frac{1}{2^{j-1}}\right) \cdot Vr\right]. \tag{25}$$

If the extra cycle occurs before the first cycle ($j = 1$), the error introduced by γ will appear at the transition points of the first-stage residue voltage and will be similar to an interstage amplitude mismatch. It will also be multiplied by the cyclic conversion, resulting in an overall DNL error of

$$\Delta_{\gamma E2(j1)} = \gamma \cdot 2^n. \tag{26}$$

However, if this operation is done before the second cycle ($j = 2$), the overall error will be bigger because a doubling operation is done before. We obtain

$$\Delta_{\gamma E2(j2)} \cong \gamma \cdot 3 \cdot 2^{n-1} = 1.5 \cdot \Delta_{\gamma E2(j1)}. \tag{27}$$

The minimal error is therefore obtained when the extra cycle is performed before the first conversion cycle. This extra cycle operation also introduces errors in the cyclic conversion: When inserted before the first cycle, it produces a major error at the MSB transition corresponding to codes $[0,0,1,0,\ldots,0]$ and $[1,-1,-1,0,\ldots,0]$. The residue voltage for these two values can be computed, and the difference gives the introduced error at this point

$$\Delta_{\gamma E1(j1)} \cong \gamma \cdot 3 \cdot 2^{n-2}. \tag{28}$$

This error is smaller than the error introduced at the first-stage residue voltage transitions. If the extra cycle is done before the second cycle, the major error appears at voltages $\pm Vth/2$ (i.e., $\pm Vr/8$). The critical codes are $[0,0,0,1,0,\ldots,0]$ and $[0,1,-1,-1,0,\ldots,0]$, and the error is as follows:

$$\Delta_{\gamma E1(j2)} \cong \gamma \cdot 3 \cdot 2^{n-3}. \tag{29}$$

Parameter δ also plays a role during the extra cycle. Its effect is similar to a supplementary cyclic conversion cycle.

C. First-Order Implementation

As expressed in (2), the residue voltage of a first-order incremental ADC has the appearance of a periodic falling ramp. Parameter α affects Vin only, modifying the dynamic range of the conversion but not its linearity. Parameter β increases the amplitude of the residue, thus contributing to the interstage amplitude mismatch with a positive DNL located at the transition points of the residue voltage $Vout$, multiplied by the cyclic gain 2^n of the second stage

$$\Delta_\beta = \beta \cdot 2^n. \tag{30}$$

D. Second-Order Implementation

Since the same second stage (cyclic RSD ADC) is used, it introduces the same DNL errors as for the first-order implementation. Let us now consider the influence of parameters α_1, α_2, β_1, and β_2. Parameter α_1 influences only Vin and does not contribute to nonlinearity. Due to the presence of the second integration loop, any DNL of the first integration loop will be multiplied by the integration factor $2^{k/2}$ of the second loop (cumulative effect). As for the first-order implementation, a positive DNL due to β_1 occurs at the transition points of the first residue voltage $Vout1$. This error is multiplied by $(1+\alpha_2) \cdot 2^{k/2}$ and by the gain 2^n of the second stage

$$\Delta_{\beta 1} = \beta_1 \cdot (1+\alpha_2) 2^{k/2} \cdot 2^n \cong \beta_1 \cdot 2^{n+(k/2)}. \tag{31}$$

Following the same interstage amplitude mismatch analysis, parameter α_2 of the second integrator stage, because of its amplification effect, also produces a positive DNL which is multiplied by the subsequent stage gains

$$\Delta_{\alpha 2} = \alpha_2 \cdot 2^{n+(k/2)}. \tag{32}$$

Finally, parameter β_2 introduces a negative DNL, which is also amplified by the integrator

$$\Delta_{\beta 2} = -\beta_2 \cdot 2^{n+(k/2)}. \tag{33}$$

TABLE I
SUMMARY OF LINEARITY ERRORS

Position	Linearity Errors (LSB) 1st order incremental conversion	2nd order incremental conversion
In the cyclic conversion	$\gamma \cdot 3 \cdot 2^{n-2}$	$\gamma \cdot 3 \cdot 2^{n-2}$
At each residue transition of the 1st stage	$(\beta+\gamma-\delta)\cdot 2^{n}$	$(\gamma-\delta)\cdot 2^{n}$
Middle of input range	-	$(\alpha_2+\beta_1-\beta_2)\cdot 2^{n+(k/2)}$
Other residue transition positions	-	$(\alpha_2+\beta_1)\cdot 2^{n+(k/2)-1}$ $(-\beta_2)\cdot 2^{n+(k/2)-1}$

These three errors (31)–(33) do not appear systematically on all transition points of the first integrator residue voltage. The biggest appears at the middle of the dynamic input range, which corresponds to the threshold of the comparator, while the others appear at all the other residue voltage locations with unequal values due to the compensation phenomena between α_2, β_1, and β_2.

E. Summary of the Errors and Comments

The theoretical linearity errors of the proposed hybrid ADC are summarized in Table I. For the first-order implementation, error parameters β, γ, and δ contribute each to the same error at the first-stage residue voltage transitions. Interestingly, β, γ, and δ can cancel each other. They can therefore be grouped into the same parenthesis. Parameter γ gives rise to a slightly smaller error at the second-stage MSB transition points.

For the second-order implementation, errors α_2, β_1, and β_2 are dominant because they are multiplied each by $2^{k/2}$. They constitute the fundamental resolution limitation of the proposed structure. Again, due to their position in the conversion flow, the α_2, β_1, and β_2 errors at the middle point input range can be canceled with appropriate values. Errors related to β_2 appearing in other positions of the dynamic range are different in terms of position and amplitude compared with errors due to α_2 and β_1. Therefore, they are not grouped in the summary table.

F. Simulation Results

A model of the proposed hybrid ADC, incorporating the nonidealities used in the aforementioned theoretical analysis, was used for computing the maximal achievable resolution of the first- and second-order conversion principles as a function of three different error Gaussian distributions with standard deviations of 0.1%, 0.3%, and 1% on all parameters α_1, β_1, α_2, β_2, γ, and δ. The equations described previously were implemented and simulated with Matlab. An input sinewave was applied to the converter, and the result was analyzed with a 4096-point fast Fourier transform (FFT). The effective number of bits of the converter was deduced from the signal-to-noise-and-distortion ratio computed from the FFT. Fifty runs, each of them with different randomly distributed errors, were performed for each configuration of resolution and each of the three standard deviation levels.

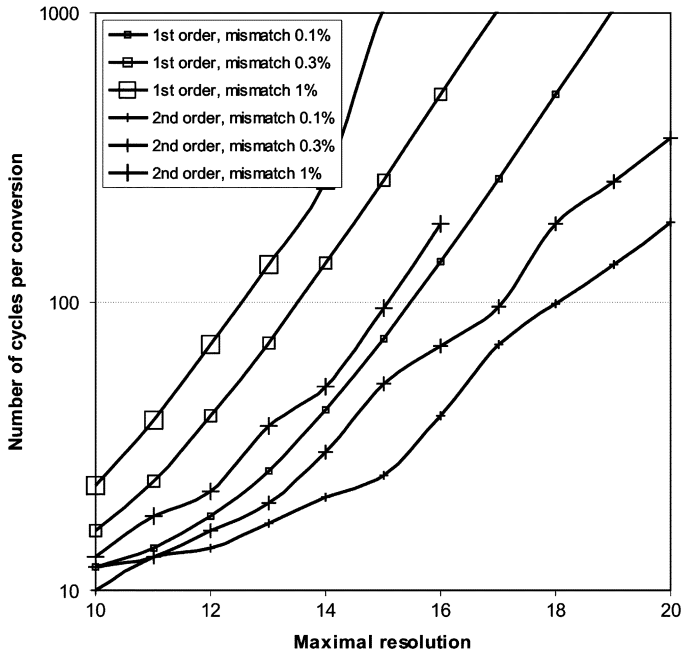

Fig. 7. Maximal achievable resolution and corresponding number of cycles per conversion for the proposed principle (first and second orders) when three different error variances of 0.1%, 0.3%, and 1% are applied to parameters α_1, β_1, α_2, β_2, and δ.

TABLE II
OPTIMAL ADC STRUCTURE AS A FUNCTION OF REQUIRED RESOLUTION AND ERROR LEVEL (SECOND-ORDER IMPLEMENTATION)

	Error Structure	0.1 % Cycles	Error Structure	0.3 % Cycles	Error Structure	1 % Cycles
12	4-8	14	6-6	16	10-2	36
14	8-6	24	10-4	38	12-2	68
16	10-6	40	12-4	70	15-1	185
18	14-4	134	15-3	187	--	--
20	16-4	262	17-3	368	--	--

The simulation results are shown in Fig. 7, where the number of conversion cycles as a function of the resolution is given. From all the resolution combinations between the first- and second-stage resolutions (k and n), the plotted structure is the one requiring the minimum number of cycles with a resolution reduced by only half an LSB. As the mismatch level decreases, the conversion is faster because more bits can be resolved by the cyclic stage, much faster than the incremental stage. Conversely, higher mismatch levels require more bits to be resolved by the first stage, thus leading to longer conversions.

For the second-order implementation, Table II gives the optimal ADC structure (parameter pair $k-n$) and the corresponding number of conversion cycles given in (12) as a function of the desired resolution for the three different error levels and for resolutions ranging from 12 to 20 b. While a 16-b conversion needs only 40 cycles with a 0.1% mismatch level, it needs 185 cycles with a 1% level. For this mismatch level, the conversion accuracy cannot be better than 16 b due to the intrinsic first-stage errors given in (31)–(33).

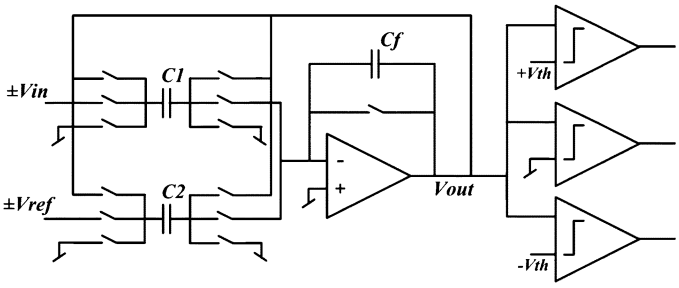

Fig. 8. Implementation example of the proposed ADC principle (first-order version): SC circuit with minimal number of components.

G. Considerations About Noise

Due to their integrating operation performed within a fixed and constant number of cycles, incremental ADCs average the internal circuit thermal noise, whose rms value is divided by the square root of the number of integration steps. For a first-order implementation, this property greatly relaxes the noise requirements of the first stage. Due to its drastically reduced number of integration steps, a second-order implementation is more sensitive to noise, compared with a first-order one. In all cases, the first stage must feature an output noise level sufficiently small so as not to affect the conversion accuracy of the second stage. Since mismatch limits the resolution of the second stage to about 8 b, its noise limit is usually not a concern for the conversion accuracy.

IV. Implementation Example

To illustrate the reduced implementation complexity of the proposed conversion principle, we present a switched-capacitor (SC) implementation of a first-order incremental converter followed by an RSD cyclic converter. The key idea of this implementation is to use the same hardware for both stages (incremental and cyclic) and operate them in a two-step conversion mode. The resulting circuit, shown in Fig. 8, is very compact and requires only one active element, three capacitors, three dynamic comparators, and switches. It can be realized using a standard CMOS process technology.

The ADC is first used in incremental mode. For this, in a first step, capacitor $C1$ is charged with input voltage Vin, and the charge is transferred to the feedback capacitor Cf. In a second step, capacitor $C2$ is charged with reference voltage $+Vr$ or $-Vr$ (depending on the result of the comparator connected to ground), and the charge is also transferred to Cf. These steps are repeated $p+1$ times. Then, with a special switching technique [10], the residue voltage on $Vout$ is inverted and copied into Cf. The inverted input is again integrated $p+1$ times. The first k bits are obtained, as well as a residue voltage on $Vout$.

Then, the same hardware is switched to a cyclic RSD converter to perform the second part of the conversion. First, the residue voltage $Vout$ is sampled into the two input capacitors $C1$ and $C2$. Then, their charges are transferred to Cf, and the reference voltage operation is applied to capacitor $C2$ (depending on the ternary result of the comparators connected to $+Vth$ and $-Vth$, being roughly $+Vref/4$ and $-Vref/4$, respectively). The extra cycle can be easily implemented by using only one capacitor during the sampling of the input voltage, to provide a multiplication by one instead of two.

TABLE III
Comparison of the Proposed Conversion Principle With First- and Second-Order Incremental Converters for a 14-Bit ADC

	Structure		
	Incremental 1st order	Incremental 2nd order	Proposed scheme
Linearity error (LSB)	< 0.1	< 0.1	0.4
Number of cycles	8196	130	73

Matlab simulations of the proposed converter were carried out to evaluate its resolution, based on charge transfer equations and on the same methodology as in Fig. 7. The following nonideality conditions were used:

1) mismatch of 0.3% (standard deviation) for all capacitors;
2) random offset associated to the OTA amounting to 1% of the input dynamic range;
3) random white noise in the comparators amounting to 3% of the input dynamic range;
4) parasitic capacitor of 20% on all capacitors;
5) limited gain of the OTA to 80 dB.

The simulated performance of the implementation example featuring 14 b of resolution (6 b in the first stage and 8 b in the second stage) is compared with the simulated performance of the first- and second-order incremental ADCs with the same resolution (Table III). The benefits in speed are clearly demonstrated: Compared with a first-order incremental ADC, the number of cycles is divided by 113, while having the same hardware. Compared with the second-order one, the number of cycles is divided by 1.8, and the hardware complexity by a factor of two.

V. Conclusion

A new hybrid ADC principle, based on the association of an incremental conversion (first or second order) for the most significant part of the result and on a cyclic conversion for the least significant part, has been presented. A theoretical analysis of the conversion accuracy has been provided, based on mismatch considerations. The flexibility in distributing the overall resolution between the two stages allows an optimized operation for each resolution regardless of the mismatch level. A disadvantage of this principle is a poorer antialiasing filtering property compared with that of sigma–delta ADCs.

Simulation results show that the proposed first-order conversion principle is much faster than an equivalent first-order incremental (typically 100 times faster) or first-order sigma–delta ADC (typically ten times faster). For resolutions up to 14 b, it can even compete with a second-order sigma–delta solution, while needing half of its hardware complexity, making it suitable for medium-resolution, ultrasmall, and ultralow-power ADCs. Regarding the proposed second-order implementation, it can compete in speed with a third-order sigma–delta ADC up to resolutions of 16 b, while showing a smaller complexity and an inherent stability.

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