A Subthreshold SCL Based Pipelined Encoder for Ultra-Low Power 8-bit Folding/Interpolating ADC

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***Abstract*- The subthreshold MOS source-coupled logic (STSCL) technique is of great interest for designing ultra low power circuits. In this paper we discuss the design of a pipelined encoder for an 8-bit folding and interpolating (F&I) analog-to-digital (ADC) data converter using this technique. The encoder is designed and characterized in a conventional 0.18µm CMOS technology, and it is capable of operating over a wide frequency range (10kHz-50MHz) without the need of resizing the transistors or scaling the voltage levels. The speed and power consumption of the encoder are proportional to the bias currents of the gates. The supply voltage of the circuit can be as low as 350mV.**

I. INTRODUCTION

Source-coupled logic (SCL) or MOS current-mode logic (MCML) circuits are emerging as a promising technique for high performance and low power designs [1][2]. SCL circuits benefits from immunity to noise and crosstalk, low swing voltage and insensitivity to process variations. In comparison with traditional CMOS designs, SCL circuits continuously dissipate a constant current, however, this topology is very desirable for some applications in mixed signal environments [1], especially when low switching noise is required. The recently proposed STSCL technique [2] takes advantage of SCL circuits while offering an effective way to design ultra low power circuits in subthreshold regime. One interesting aspect of STSCL circuits is that the speed and power consumption of the circuits can be simply adjusted linearly by altering the amount of bias current without the need to resize the devices. This property makes these circuits very interesting for applications where a wide range of operation frequency is required.

In this work we demonstrate the design of a pipelined encoder for an 8-bit F&I ADC using the STSCL technique. F&I ADCs are used to digitize the high-bandwidth signals at low-to-medium resolution [3]. The motivation to use an F&I ADC rather than a flash ADC is that the number of the comparators in design (and hence the area and the power consumption) is reduced dramatically which is essential for low power applications.

This paper is organized as follows. Design of the STSCL circuits, sizing methodology and stacking effects are discussed in Section II. We present the detailed design of the basic building blocks for the pipelined encoder in Section III. Section IV presents the simulation results and finally, the conclusion is presented in Section V.

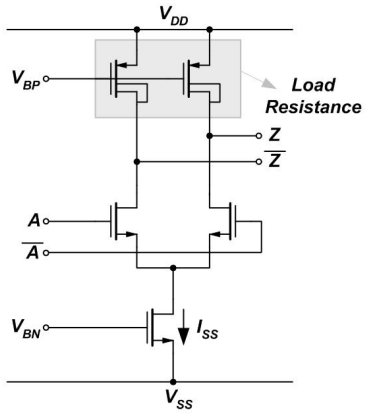

Fig. 1. Schematic of a buffer/inverter designed using the STSCL technique.

II. SUBTHRESHOLD MOS CURRENT-MODE LOGIC

An SCL circuit consists of a constant current source, one or multiple source-coupled nMOS differential pair(s) and the loads. The differential pair switches the constant current between two branches and the load converts the current to output voltage. The speed of switching can be very high and is proportional to the amount of the bias current. Note that the voltage swing at the output should be large enough otherwise the differential pairs of the next stage cannot completely switch the current. In STSCL circuits, the source-coupled nMOS differential pairs are biased in weak inversion (WI) and hence the swing voltage should be larger than about $4\times nU_T$ where n is the subthreshold slope factor for nMOS devices and U_T is the thermal voltage. The load in an STSCL circuit is a pMOS transistor where the bulk terminal is connected to the drain. This device is also biased in WI and provides a large equivalent resistance [2].

A. Sizing Considerations

For transistor sizing, we study a simple buffer/inverter designed using the STSCL technique which is shown in Fig. 1. The bias current (I_{SS}) is chosen based on the trade off between the power consumption and the speed of the circuit. An nMOS device which is biased in strong inversion provides this current. The bias current can be altered by adjusting the bias voltage of the nMOS device (V_{BN}). An advantage of designing circuits using STSCL technique is that these circuits can operate in a wide range of bias current. When the bias current is altered, all devices which switch the current should remain

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in WI for proper operation. Based on the EKV model [4], the dimension of the nMOS devices is determined by:

$$W / L = I_{Bias,MAX} \big/ (2 \times n.\mu_n .C_{ox} .IC.U_T^2) \quad (1)$$

where μ_n is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area and IC is the device inversion coefficient. After choosing an appropriate value for the bias current, the bias voltage of the pMOS devices (V_{BP}) should be fixed to provide the desired swing voltage at the output. A variable swing controller can be used for this purpose which enables the circuit to operate with different bias currents. An example of a general variable swing controller is given in [5].

B. Stacking Effects

Design of logic circuits using STSCL technique sometimes requires having one or multiple stacks of transistors in the nMOS networks. The reason for stacking is to avoid implementing the logic using multiple cascaded gates which increases the area and power consumption of the circuit. In conventional current mode logic designs, connecting several transistors in a series stack may need careful resizing of the transistors or using level shifters but this is not the case for the STSCL technique. The gate transconductance in weak inversion is given by [4]:

$$G_m = I_D / (n.U_T) \quad (2)$$

where I_D is the drain current. The gate transconductance in WI is independent of the input gate to source voltage and hence as long as nMOS devices are operating in WI, they can switch the current and the logic evaluation will be performed correctly. Considering the same dimension (W/L) for all the transistors in a stack, a stack of N nMOS devices can be modeled as a single device with the dimension (W/(N×L)). Figure 2 shows the schematic of a stack of N conducting transistors and its equivalent model. Only the half circuit which is conducting is shown in this figure. Taking (1) for the modeled device into account will lead us to the fact that for a fixed inversion coefficient, the maximum bias current that guarantees the operation of the devices in WI becomes lower by a factor of N. Since the switching speed of the STSCL circuits is proportional to the bias current, the reduced maximum bias current results in a lower maximum operation speed. This reduced maximum speed is not critical because the aim of STSCL technique is to design low power circuits. In the next section, we will discuss the design of an 8-bit F&I ADC using the STSCL technique.

III. CIRCUIT DESCRIPTION

A. Encoder Topology

The block diagram of an F&I ADC is shown in Fig. 3. There are two signal paths in this architecture: the coarse and fine paths. These paths generate the coarse and fine bits which are then converted to binary bits using an encoder. The coarse bits are simply generated using a simple 3-bit flash quantizer. Generation of the fine bits involves designing the folders, interpolators and current comparators. Use of the folders reduces the number of the comparators by the folding factor.

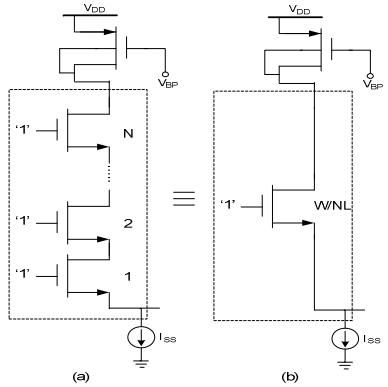

Fig. 2. (a) Schematic of the nMOS network with a stack of N conducting nMOS devices all biased in WI. (b) Equivalent model of the conducting devices in stack.

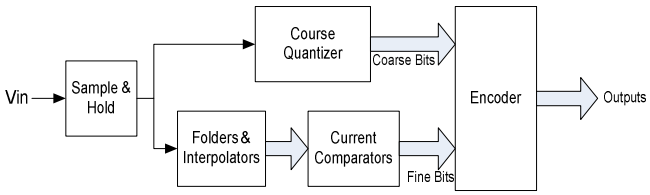

Fig. 3. Block diagram of an F&I ADC.

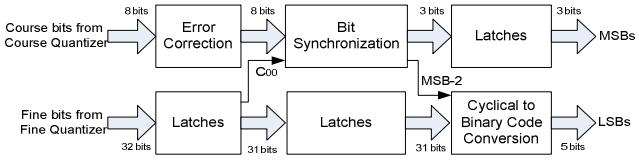

Fig. 4. Block diagram of the pipelined encoder for an 8-bit F&I ADC [3].

The interpolation is employed to reduce the number of the folding amplifiers which reduces the area and cost of the circuit significantly. Design of the folders and interpolators is discussed in [3]. Figure 4 shows the block diagram of the pipelined encoder for the 8-bit F&I ADC. To reduce the number of the latches in the design, each gate in the pipelined encoder evaluates its outputs during half period of the clock signal and then latches the results during the other half period (see Fig. 5). An error correction circuit has been utilized in the coarse path to achieve a lower bit error rate [6]. The cyclical code to binary code converter first converts the fine bits to Gray code to correct the bubble errors in the fine path and then converts the gray code to binary code. Hence there is no need to a separate error correction in the fine path.

Bit synchronization is one of the main problems of F&I ADCs since the coarse and fine bits are generated using different paths. A bit synchronization scheme is employed in the course path to synchronize the generation of the course and fine bits. The synchronization bit in the Fig. 4 is C_{00} which is generated by the fine quantizer. The synchronized LSB output of the bit synchronization block is then used by the cyclical to binary code conversion block to convert the fine bits to binary codes. During error correction and bit synchronization intervals, the fine bits are latched. The following sections discuss design of the encoder's basic building blocks in detail.

B. Error Correction

Comparator metastability, threshold voltage variations, device mismatches and other interference may cause unwanted zeros at the output of the comparators which are called bubble errors [6]. An error correction circuitry is used in the course path to reject the bubble errors. The error correction block in Fig. 4 consists of 8 latched majority cells. The output of a majority cell is at logic '1' when at least two out of the three inputs are at logic '1'. Figure 5 shows the schematic of the latched majority cell. The current source was realized using a cascode current mirror.

C. Bit Synchronization

Synchronizing the generation of the coarse and fine bits is an important issue in the design of an F&I ADC due to different paths for the fine and course bits. A small timing mismatch between the coarse and fine quantizers can cause nonlinearity error. The bit synchronization block in Fig. 4 uses 8 cycle pointers (CP1-CP8) and the synchronization bit (C_{00}) to generate 3 MSBs. Cycle pointers are basically the outputs of the flash quantizer that after error correction are fed to the bit synchronization block. Figure 6 shows the waveforms of the bit synchronization block. The equations for generating MSB, MSB-1 and MSB-2 are:

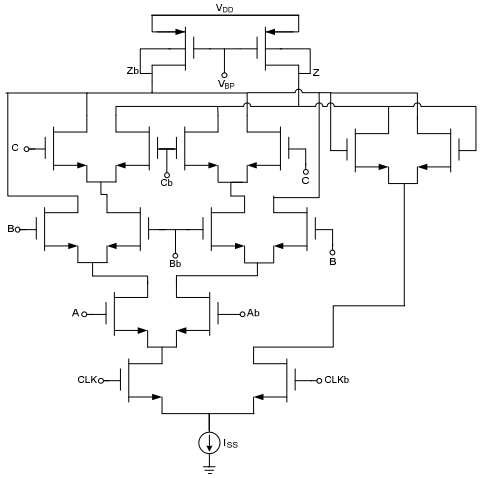

Fig. 5. Schematic of the designed latched majority cell. The gate latches the outputs when the clock signal is low.

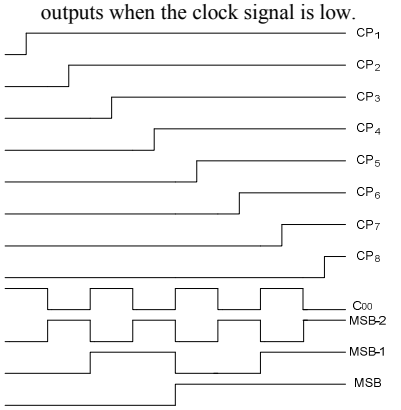

Fig. 6. Waveforms of the bit synchronization block. MSB, MSB-1 and MSB-2 are the outputs. C_{00} is the synchronization bit and CP_1-CP_8 are cycle pointers.

$$MSB = CP_5 + CP_4.C_{00} \quad (3)$$

$$MSB-1 = CP_7 + CP_6.C_{00} + CP_5'.C_{00}'.CP_3 + CP_4'.C_{00}.CP_2 \quad (4)$$

$$MSB-2 = CP_8 + CP_1.C_{00}' \quad (5)$$

All the MSBs can be simply generated only using the gates with characteristic equations of the form $Z_1=A.B+C$ and $Z_2=A.B.C$. Figure 7 shows the modified schematics of these two gates with the capability of latching the outputs. Generation of the MSB-2 does not require an additional gate for OR operation since $Z_2'=A'+B'+C'$ is also available and all the inputs and outputs are differential.

D. Cyclical Code to Binary Code Conversion

The output of the fine quantizer is called cyclical code which can be easily converted to binary code using XOR operation. The fine bits (31 bits) and the LSB output of the bit synchronization block (MSB-2) are the inputs of the code conversion block. Generation of the fine and coarse binary outputs remains synchronized by using the output of the bit synchronization block as an input of the converter. Fig. 8 shows the schematic of the circuit for cyclical code to binary code conversion. In fact, the cyclical code is first converted to gray code which can eliminate the bubble errors and then converted to binary code using sequential XOR operation. Sequential gray code to binary code conversion uses the minimum number of XOR gates which is efficient from both the point of view of the power consumption and the area of the circuit but obviously generates the outputs with a high latency. Figure 9 shows the schematics of a latch and a latched XOR gate which were used in the design of the cyclical code to binary code conversion. The outputs of the bit synchronization block should be latched during conversion because of the pipelined operation of the encoder. These bits and the outputs of the conversion block form the outputs of the encoder.

IV. Simulation Results

The pipelined encoder has been designed in 0.18µm CMOS technology.

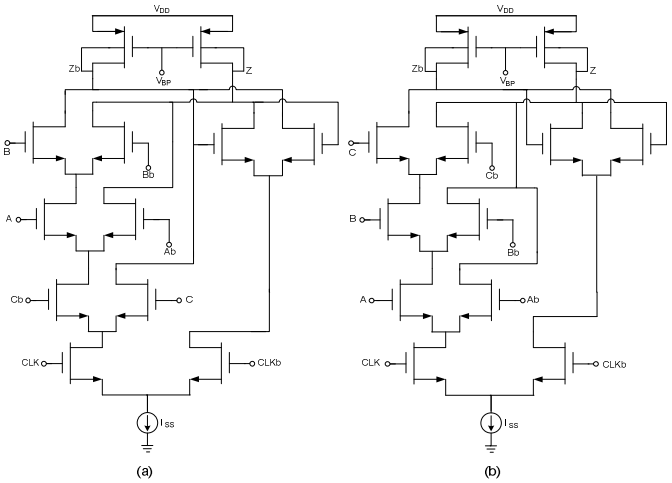

Fig. 7. Schematics of the latched gates with characteristic equations of (a) $Z_1=A.B+C$ and (b) $Z_2=A.B.C$.

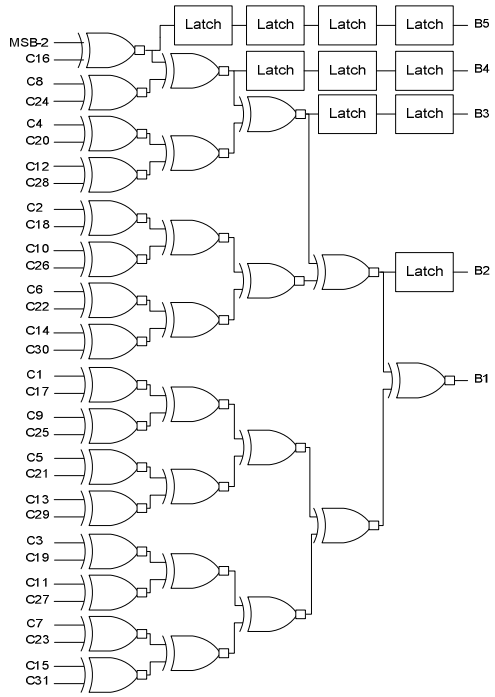

Fig. 8. Cyclical code to binary code conversion.

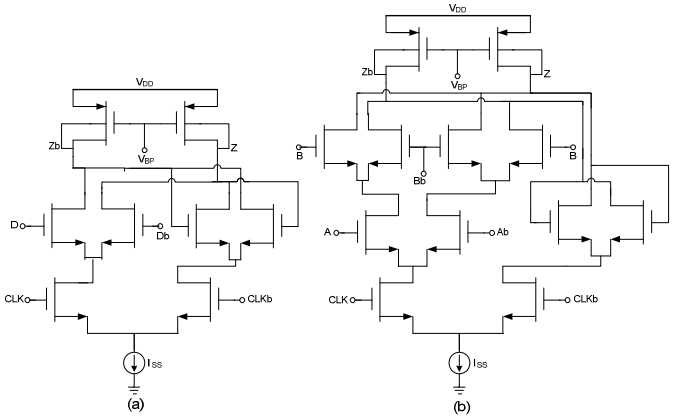

Fig. 9. Schematics of the designed (a) latch, and (b) latched XOR gates.

Simulation results show that the encoder can operate in a wide range of frequencies by adjusting the bias current of the gates. Figure 10 shows the maximum frequency of operation of the encoder for various bias currents. The supply and the desired swing voltage were 1.0V and 0.2V, respectively. The maximum frequency of operation shows a linear behavior with respect to the bias current per gate in the range of 250pA to 50nA. Further increasing the bias current brings the differential pair transistors from WI to moderate inversion which degrades the linear dependency of the frequency of operation to the bias current. Furthermore, the minimum supply voltage that the encoder can operate with depends on the bias current. The dependency is shown in Fig. 11. Increasing the bias current of the gates lowers the V_{BP} voltage. Hence, the minimum supply voltage should be increased for proper operation of the gates. At a tail bias current of 1nA and supply voltage of 1V per gate, the encoder consisting of a total of 196 gates is shown to operate at a clock frequency 100kHz with near-perfect eye opening.

V. Conclusion

A pipelined encoder for an 8-bit F&I ADC is designed using Subthreshold SCL technique. Simulation results show that the encoder can operate over a wide frequency range between 10kHz and 50MHz. The speed and power consumption of the circuit are bias dependent and can be simply adjusted by altering the bias currents of the gates. For this range of operating frequency, the power consumption varies between 20nW and 200uW. The supply voltage can be lowered until the swing voltage at the output reaches to its minimum allowed value. The circuit also generates low amplitude current spikes which does not affect the supply voltage of the circuit significantly.

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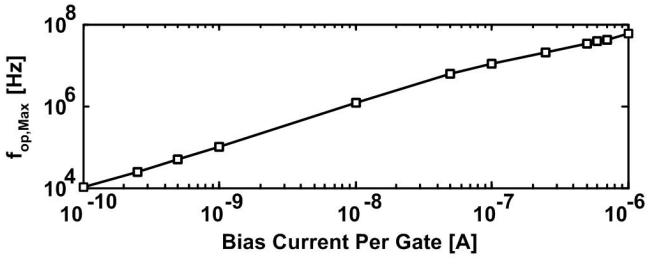

Fig. 10. Maximum frequency of operation for various bias currents per gate.

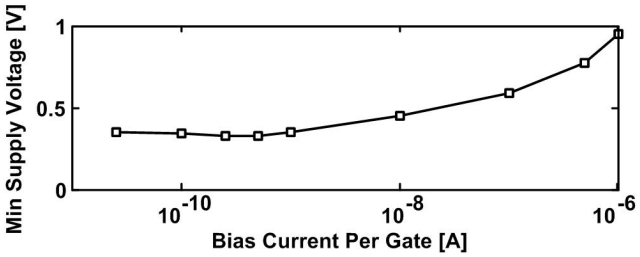

Fig. 11. Minimum supply voltage for various bias currents per gate.